Wanted: A backend transport standard for burn-in and test

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Leaders in the semiconductor industry have learned well the lessons of the learning curve that underlies *Moore's Law,* as they assiduously seek ways to accelerate their own learning curves.

Fundamentally, the business is simple: Gain a few percentage points in the slope of your learning curve and you win.

The converse is also true. At some level we all understand this, but few execute as well as Intel, a clear leader in semiconductor manufacturing. Backend packaging and test could pick up a few pointers from their wafer fab experience.

In the past several years, Intel has moved its front-end fabs to full lights-out automation to accelerate their learning curve. The benefits go well beyond scrimping on the cost of labor. As explained by Tom Franz, VP/GM of fab/sort at Intel, the focus is on tool and process learning instead of moving WIP around the line[1].

Over a two-year period, Intel improved cycle time by 50 percent, according to Franz. Over the same period, Intel improved tool utilization by 10-30 percent.

To control CAPEX, standardization of tools is essential in allowing tool reuse. We learn from this fab experience that full automation enables rapid learning and propels the industry forward.

A key enabler[2] for lights-out automation in the fab is a single wafer front-opening unified pod (FOUP), a standardized pod. Wafers are transported through the fab in the FOUP, controlled by a logistics system that keeps WIP efficiently in front of tools.

The single-wafer FOUP does not tie-up WIP sitting in a stack of wafers. Importantly, equipment suppliers can build efficient tools to one standard wafer interface, avoiding the cost, logistics problems and delays entailed in a plethora of custom fixtures and protocols.

WHAT ABOUT THE BACKEND?

So, what about backend packaging and test, which consumes an increasing share of the cost of IC manufacturing?

Some inefficiency is due to a proliferation of probers, sockets, fixtures, handlers, protocols and the handling of piece parts. However, it is not that engineering has stood still in this arena.

Efforts are made to rationalize processes and standards. A move toward wafer-level processing promises to simplify packaging. Parallel testing of chips, both memory and logic, has improved efficiency and throughput. Clearly, however, more remains to be done.

ENABLING FULL AUTOMATION

Borrowing a chapter from the fab, a standard for transport through backend burn-in and test sectors is the key to enabling full automation. A logical unit of transport is a tray with alignment features and standard sizes.

Standardized trays serve the same enabling function provided to the fab by the single-wafer FOUP. Equipment can then use standardized handing, well-suited to automation, doing away with custom fixturing and piece-part handling.

A standard TnT tray (Centipede Systems)

Furthermore, for lights-out automation, the transport must be run with virtually no maintenance and must eliminate jams, cleaning, jury-rigging and other diversions.

Test-in-Tray (TnT) can conceivably run from wafer dice through finishing, burn-in, test, trim and mark-and-pack. The process flow depends upon device type and application, but handling protocols can be standardized industry-wide.

Even burn-in, the much-reviled, no-value-added process, can be automated to test during burn-in to derive valuable test information and minimize time in a more intelligent process. Arrays of parts in trays can be moved in and out of burn-in pods automatically. Throughout this process flow there is no need for handling individual parts by humans or robots.

The adoption of TnT is moving forward in MEMS applications, where standards are needed for handling a widely diverse universe of device types. A standard tray, shown above, holds 32 MEMS devices in a tray 100mm x 240mm. Trays are adapted for the automatic handling and alignment needed in test procedures at temperatures from -65°C to +180°C.

Trays are also adaptable to device types from MEMS sensors to CSPs, BGAs and flip chips, all within the same handling standards. Access to the contact array as well as to cooling surfaces is accommodated by open top- and bottom trays. Inserts adapt the tray transport to the specific device type.

ACCELERATING THE LEARNING CURVE

TnT offers the potential of enabling full lights-out automation of burn-in and test, greatly accelerating the learning curve. The backend can be closely integrated to provide fast information feedback for rapid learning.

Lights-out production trumps the race to low-wage venues and greatly reduces waste in custom fixturing of incompatible tools. The competitive advantage of TnT is compelling.

REFERENCES

1. Presented by Tom Franz, VLSI Research webcast, 7/25/07.
2. From Allen Ibara, CEO, Phiam Inc.