Wafer Level Packaging

… The Promise Evolves

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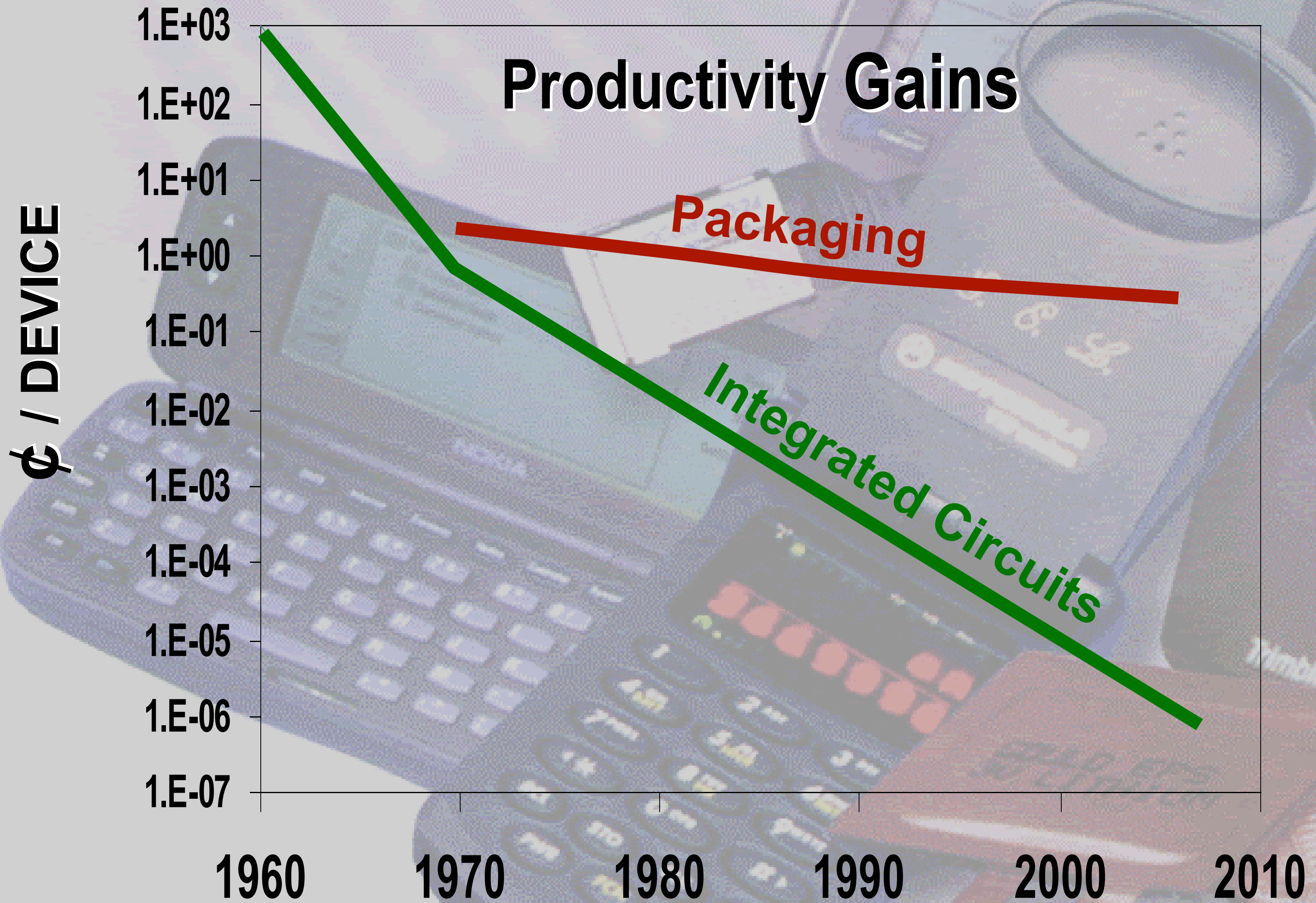
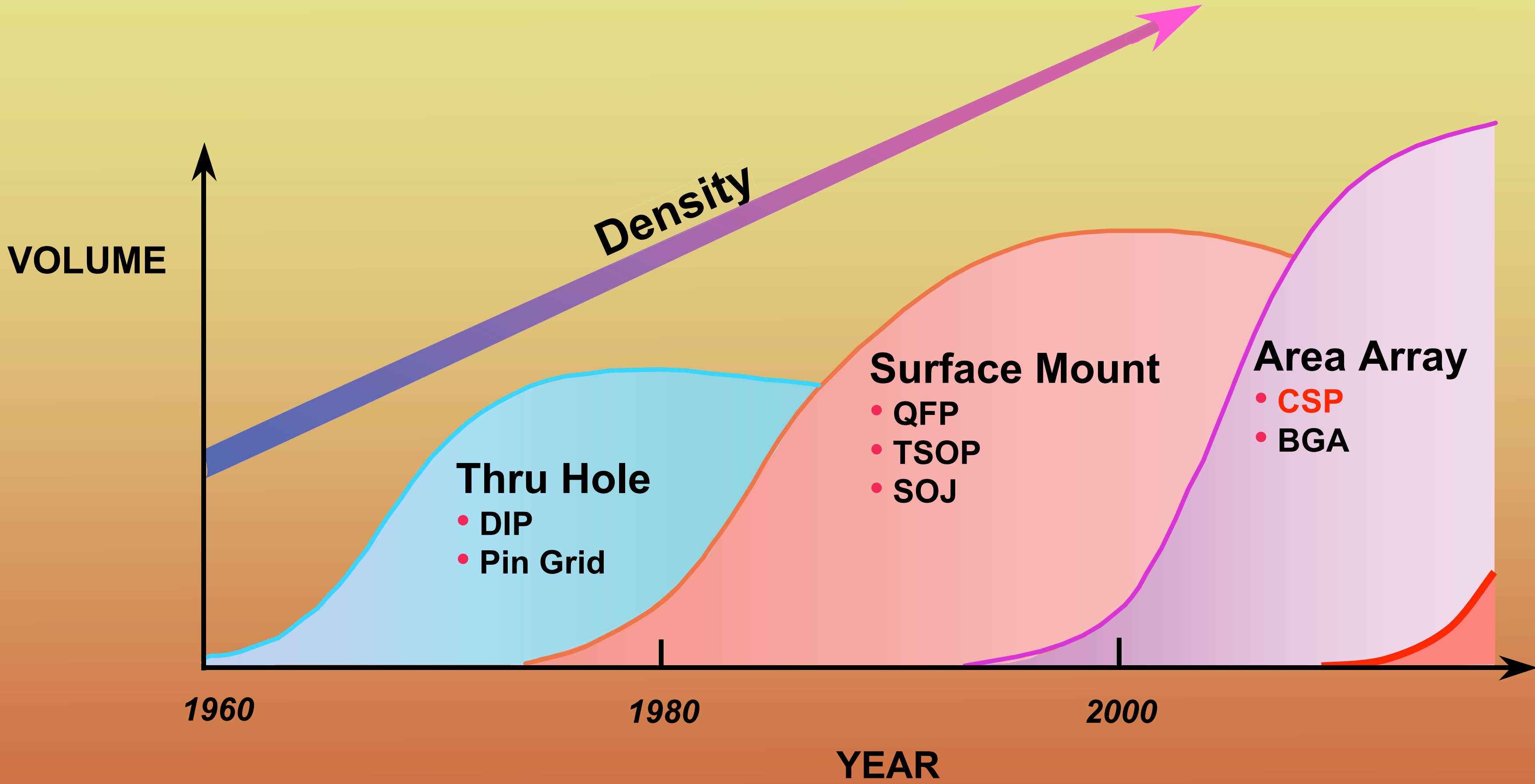
IWLPC 2008

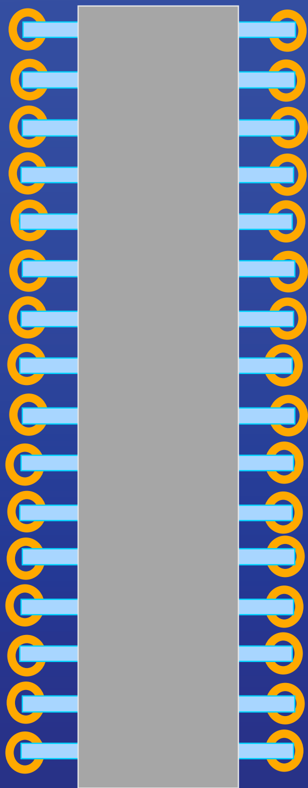

Productivity Gains
¢ / DEVICE
1.E+03
1.E+02
1.E+01
1.E+00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
1.E-06
1.E-07
Packaging
Integrated Circuits
1960
1970
1980
1990
2000
2010

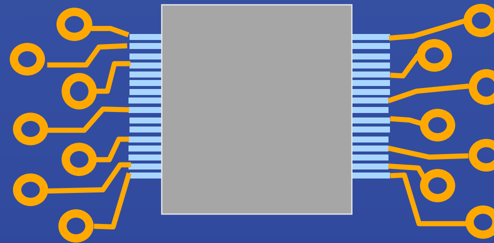
CSP-WLP Enables New Wave of I/O Density

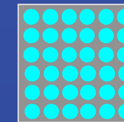


IC Packaging Progression:

Through Hole → Surface Mount → Area Array







TSOP

- 25 mil pitch
- Limited by perimeter leads

CSP / BGA

- Area array 0.8 mm to 0.3 mm
- Limited by substrate wiring
- Allows Wafer Level Processing

DIP

- 100 mil pitch
- Limited by through hole spacing

WLP is a Paradigm

Continuous Process Improvement:

- lower cost
- increased performance
- added functionality

National Semi

μSMD

Key Factors:

- Processing vs. Assembly
- Driven by cost reduction learning curve
- Applicable to diverse packaging technologies
- WLP is a process - ***Not** a package technology*

WLP Enjoys Exceptional Growth

TechSearch Projects 14% Growth (CAGR) for 2007 - 2014

- Diverse set of applications & technologies
- Growth concentrated in packages < 50 pins
- Driven by performance, form-factor (…AND COST!)

Growth in Wafer Level Packaging of MEMS Devices

- Camera chips
- Pressure sensors
- Crystal Oscillators, …

Emerging Applications in Through Silicon Via (TSV)

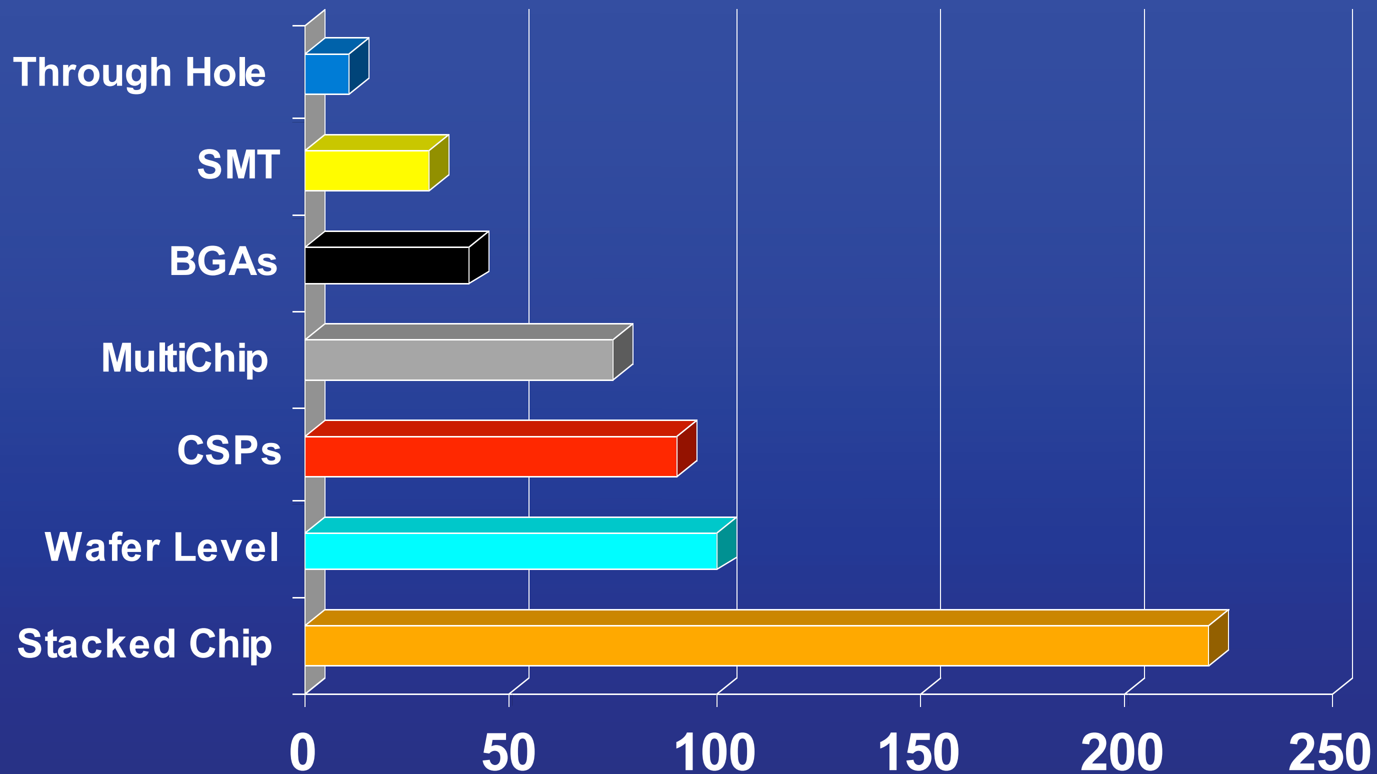
- Stacked memory

CONVENTIONAL CAMERA MODULE

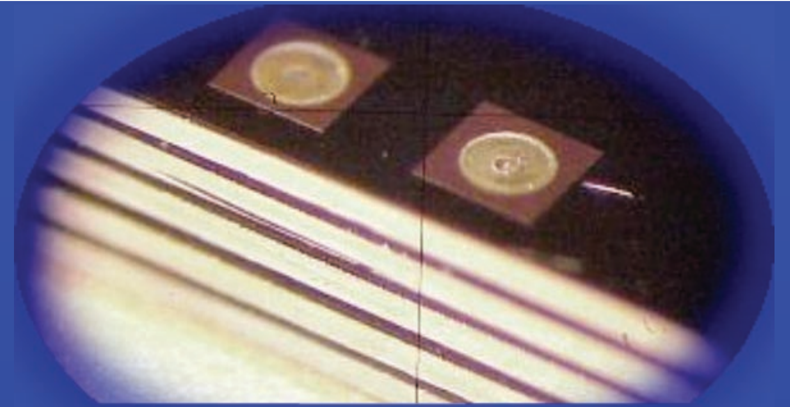
TO SCALE

Tessera iWLC

Stacked Chip Approaches are the Next Step in Density

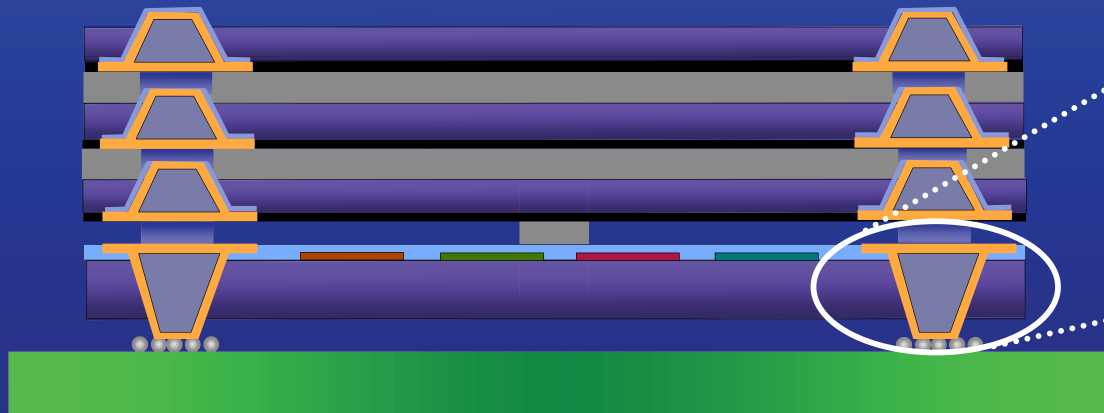


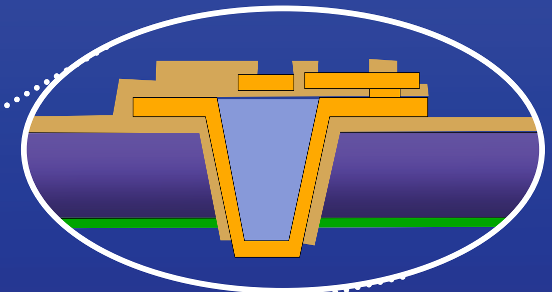
* J. Fjelstad in Electronic News 01.22.01



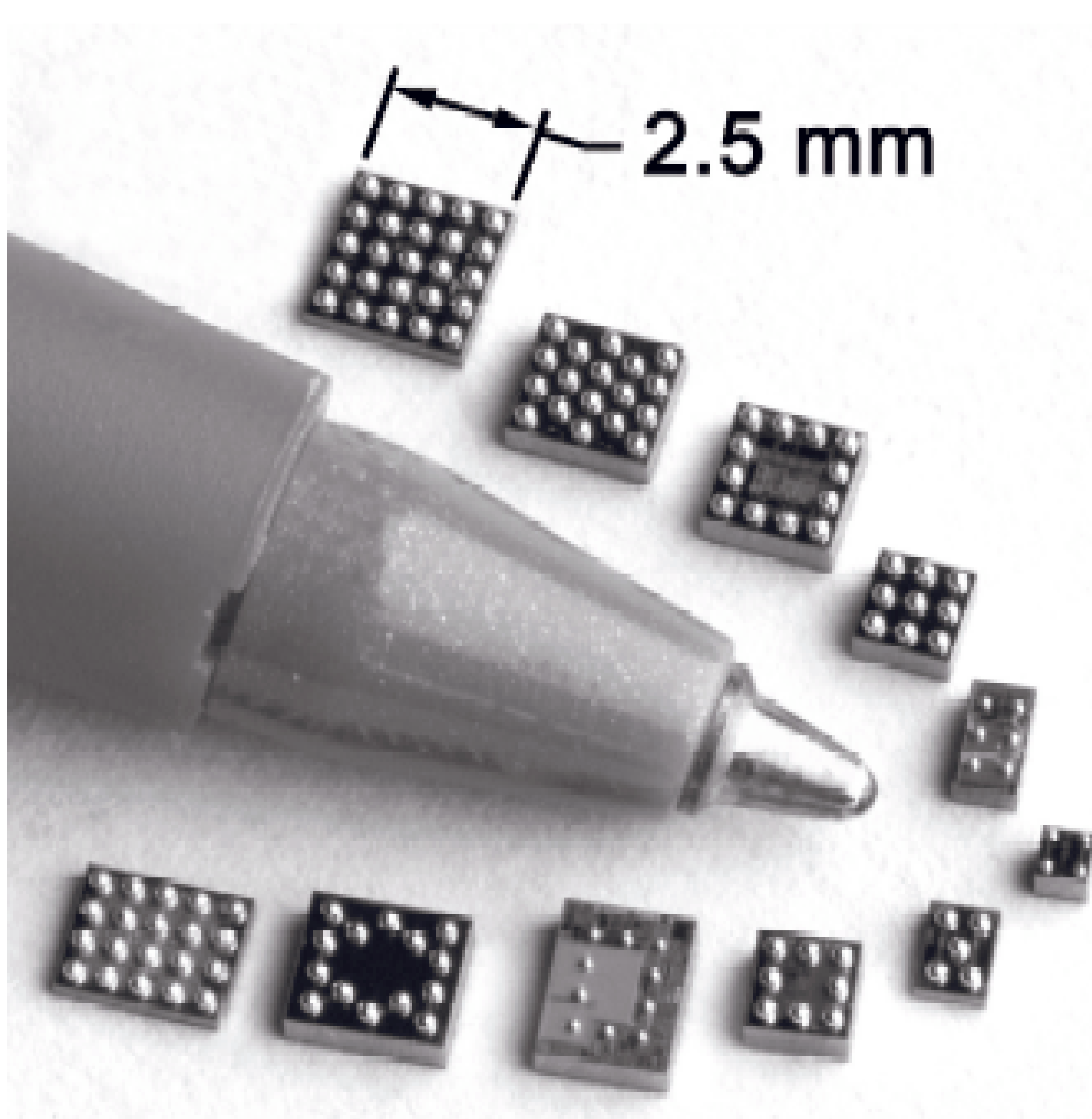
COURTESY ALLVIA

TSV (Thru-Silicon Via)





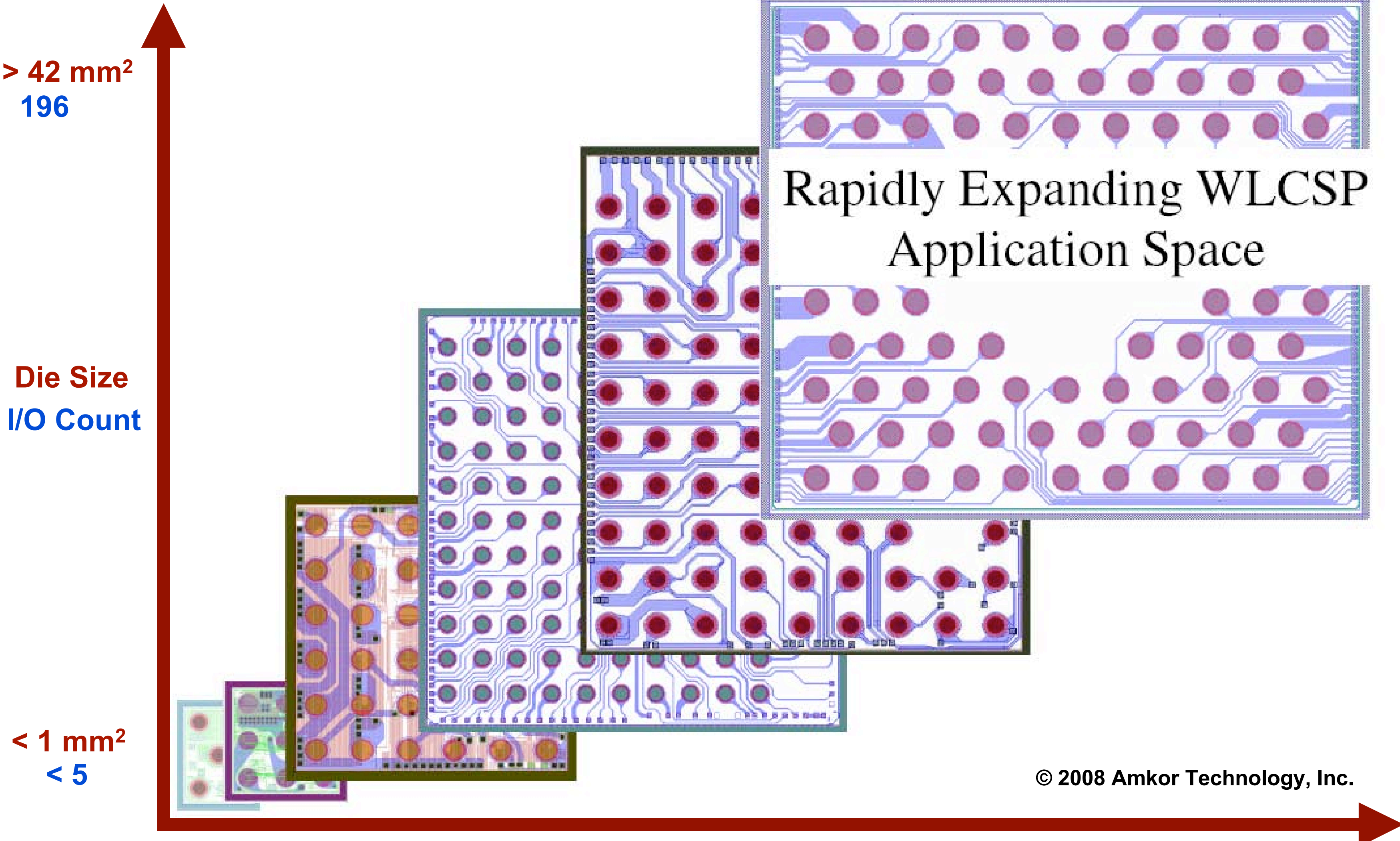
Thru Silicon-Via



Micro-SMT

National Semiconductor

Expanding WLCSP Application Space



WLCSP Market*

- Strategic and rapidly growing WLCSP business
- > 1. 3 Billion WLCSP's shipped since 2005
- >95% of WLCSP's shipped include RDL and lead free solder bumps
- Multiple customers in production, wide range of new designs in qualification
  - 0.5mm pitch dominant
  - 0.4mm pitch emerging
  - 0.3mm pitch in development
- First 300mm WLCSP qual achieved in T5 as of October 1, 2006
- Global wafer level process manufacturing footprint
  - 7 countries and 15 sites

* From Lee Smith, Amkor

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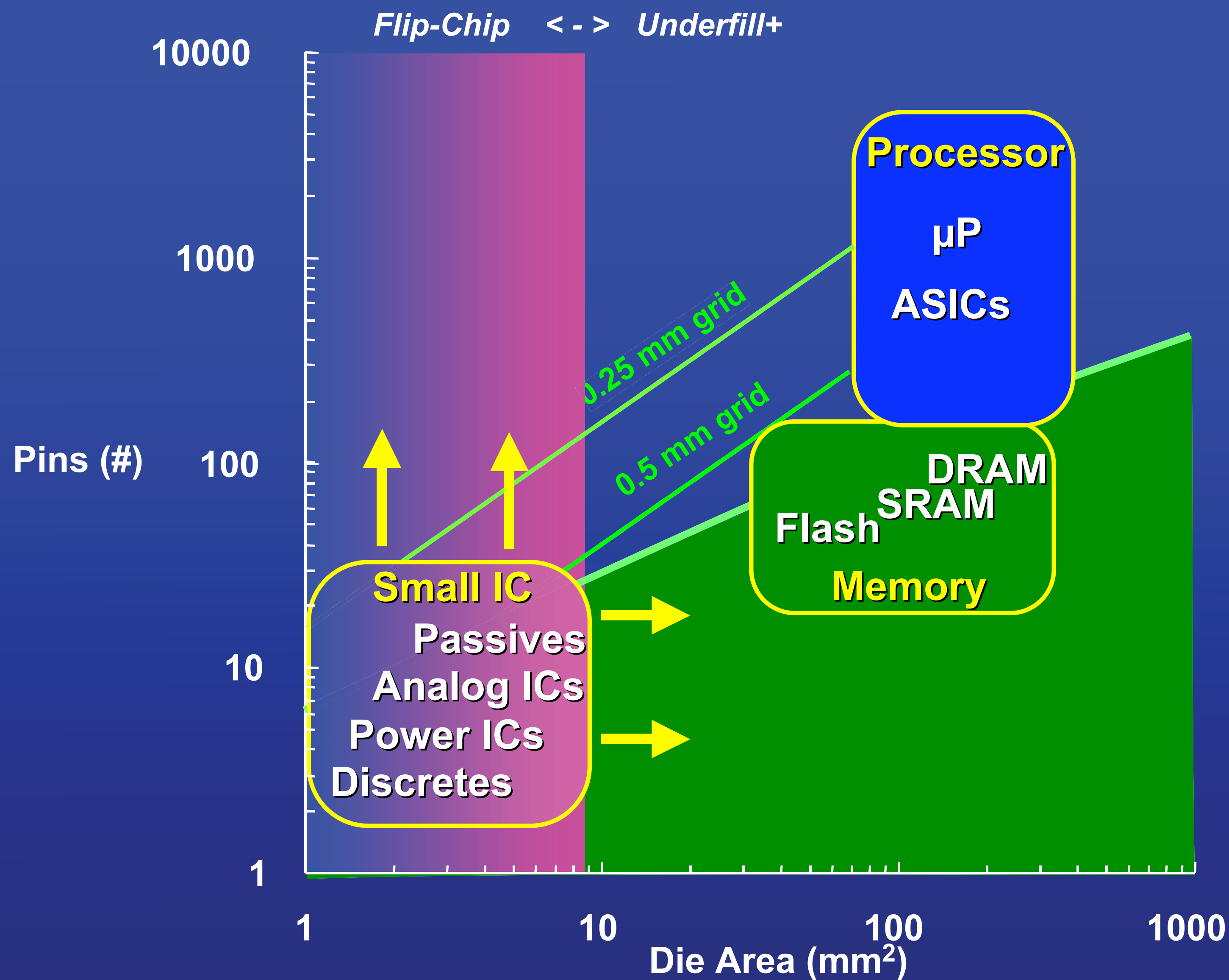


Flip-Chip < - > Underfill+
10000
1000
100
10
1
Pins (#)
1
10
100
1000
Die Area (mm^2)
Processor
µP
ASICs
0.25 mm grid
0.5 mm grid
DRAM
SRAM
Flash
Memory
Small IC
Passives
Analog ICs
Power ICs
Discretes

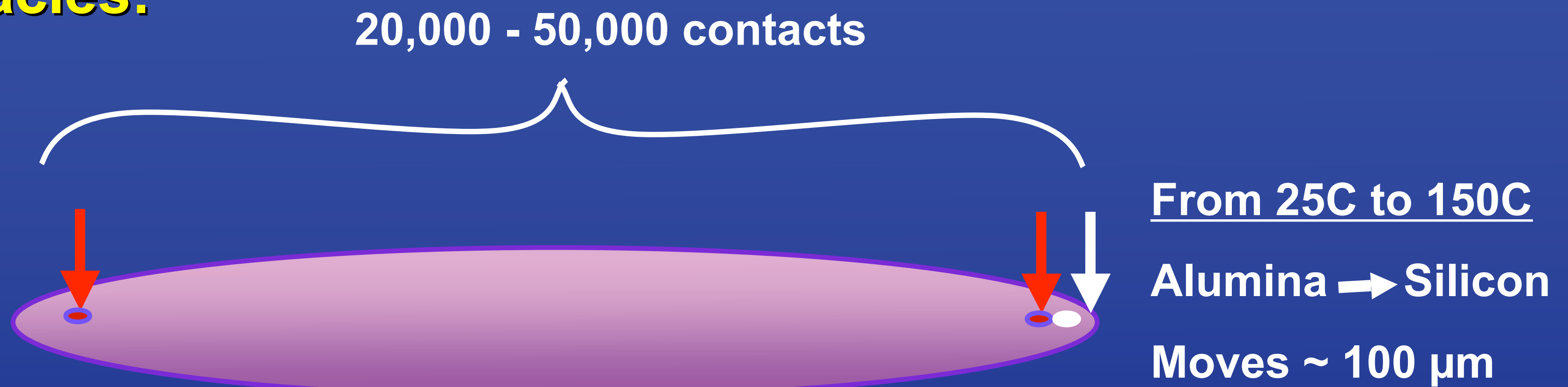
WLP has not gone Mainstream (i.e. DRAM)

WHY NOT?

- **Cost Effective Burn-in and Test**
- **Reliable Solder Attach Technology**
- **Cost!**

Full Wafer Burn-in is Stalled

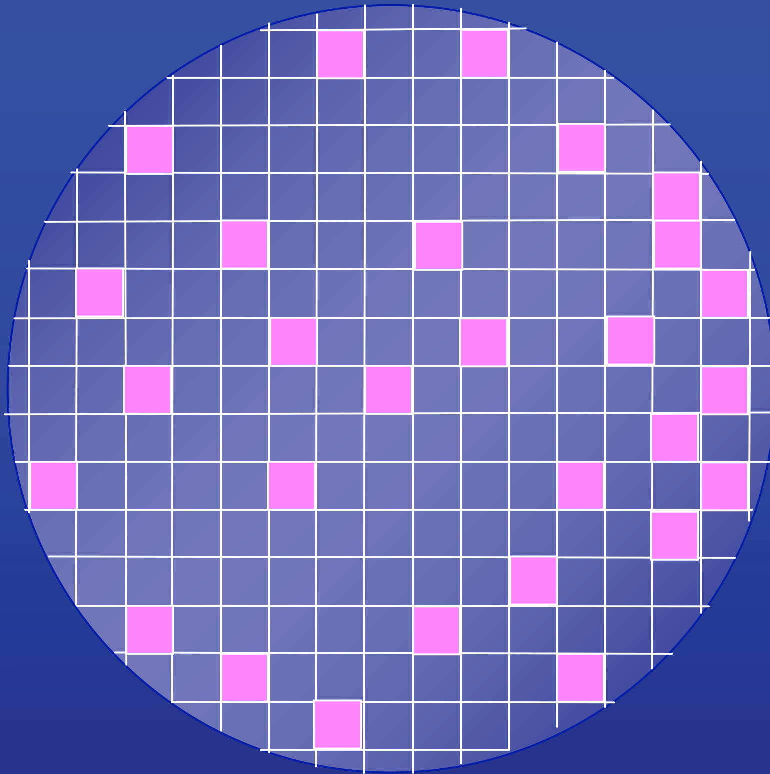
Technical Obstacles:

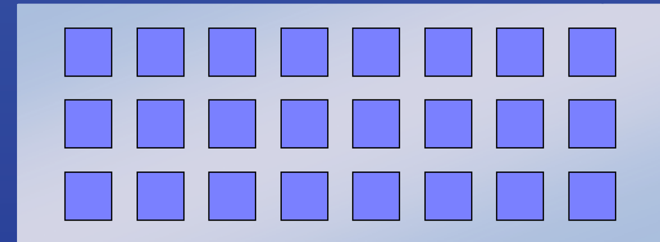


Cost: Must cost << $50,000

Equivalent to burn-in sockets & boards.

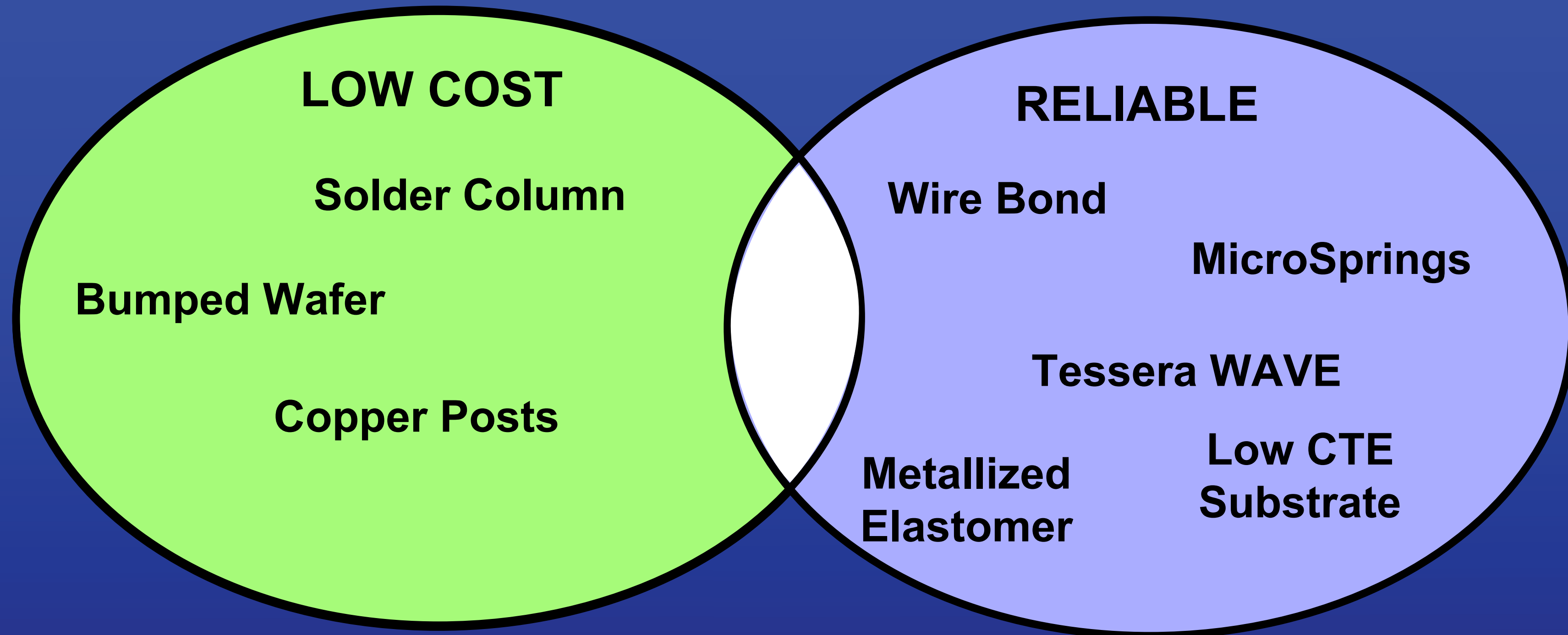
WLP Burn-in Alternatives





- **Test-in-Tray**
  - Test only good die
  - Standardized handling
  - Test and Burn-in on the same tray
  - Cost !

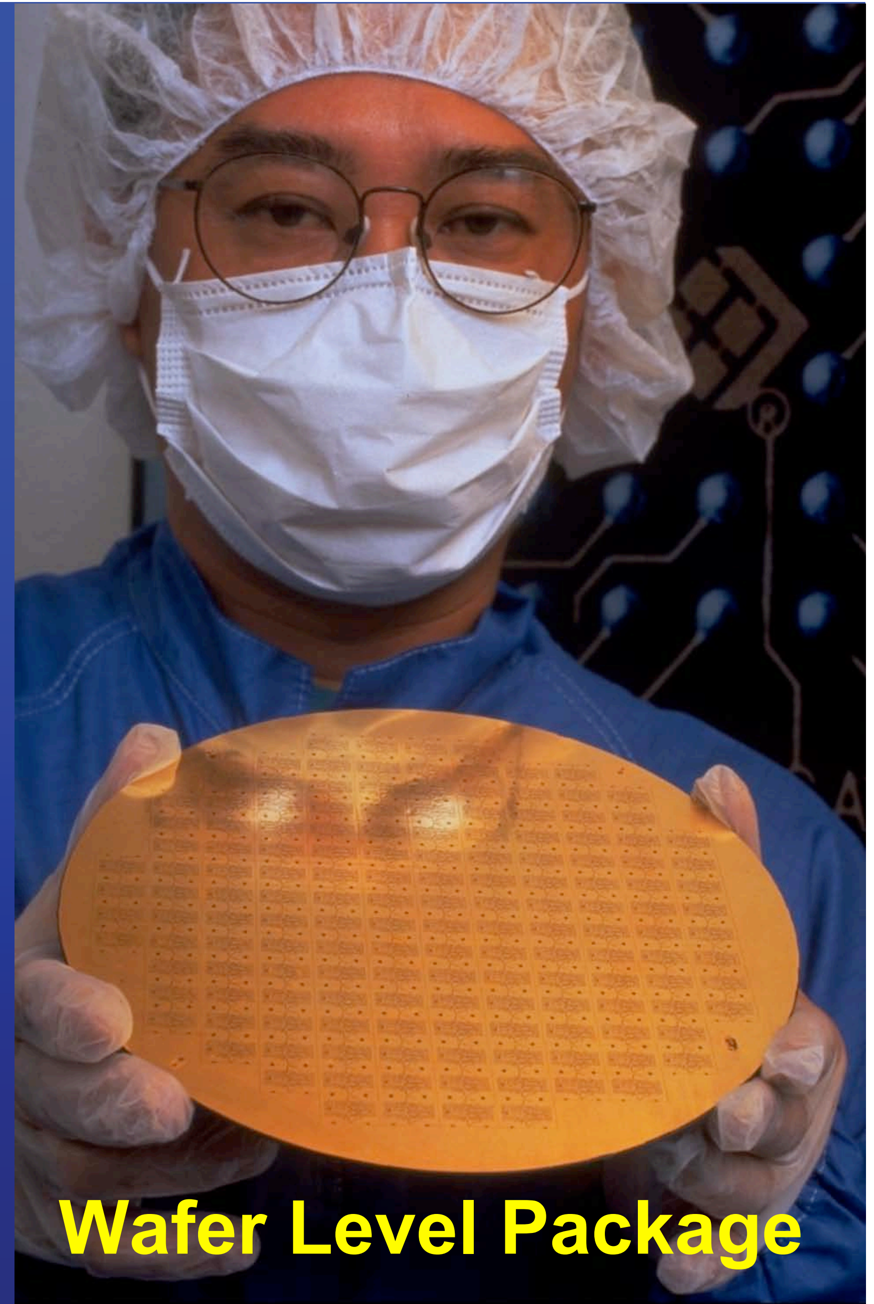
Solder Attach Technology (DRAM)



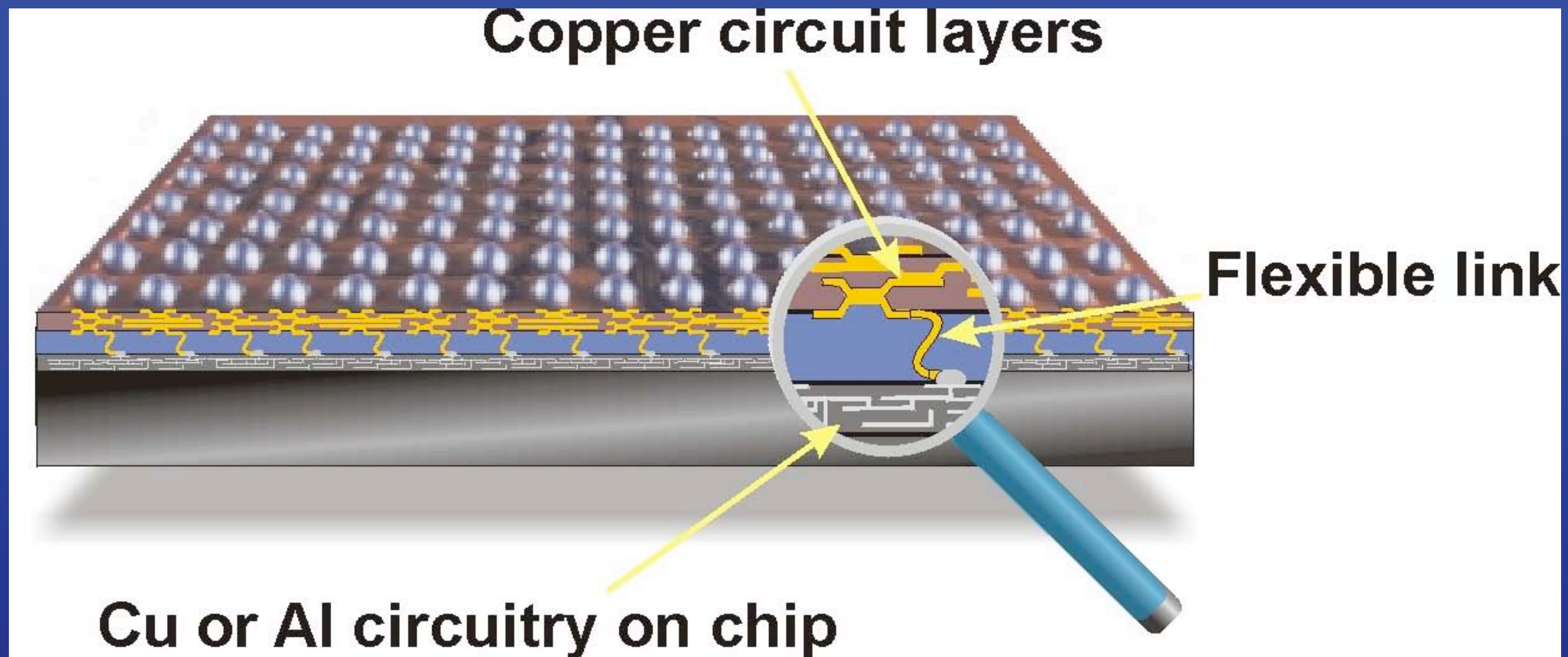
Tessera WLP

- Full wafer
- Reliable solder attach
- Power and Ground
- Wiring layers are possible

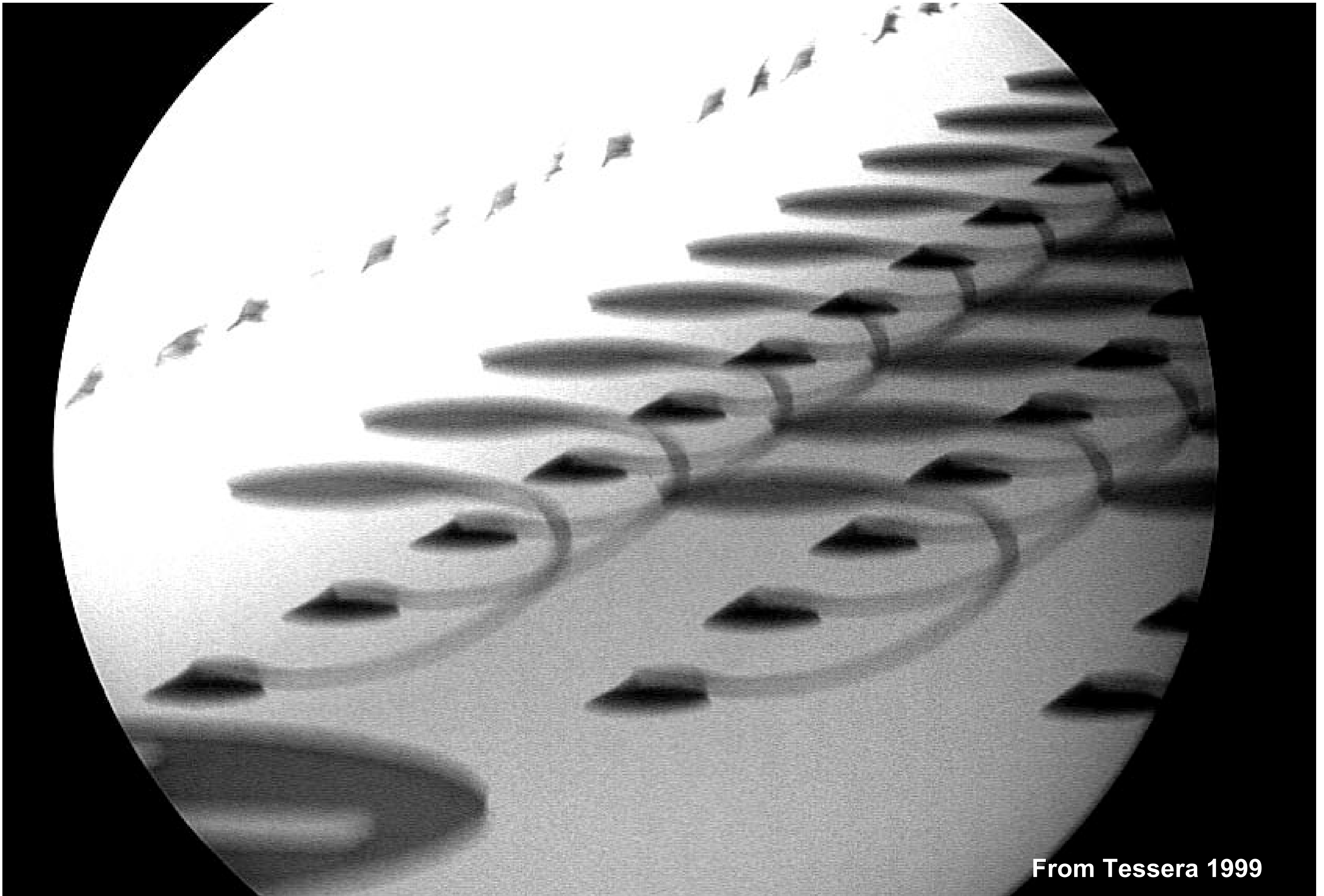
From Tessera 1999



Typical WAVE Package



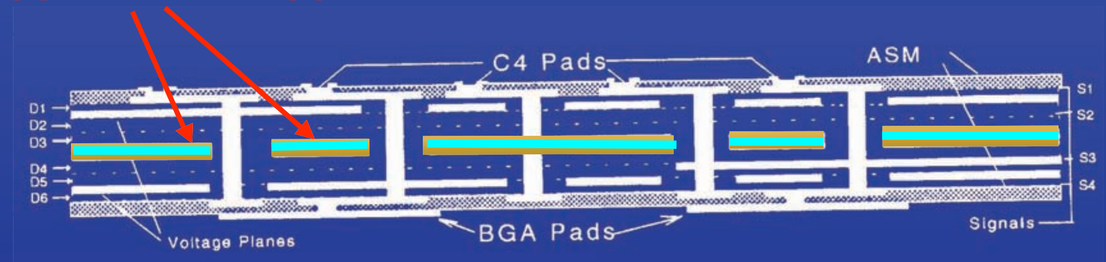
From Tessera 1999


From Tessera 1999

Low Expansion Substrate Reduces Thermal Mismatch

- **Low CTE micro-Via Boards**
- **CIC Core Substrate**

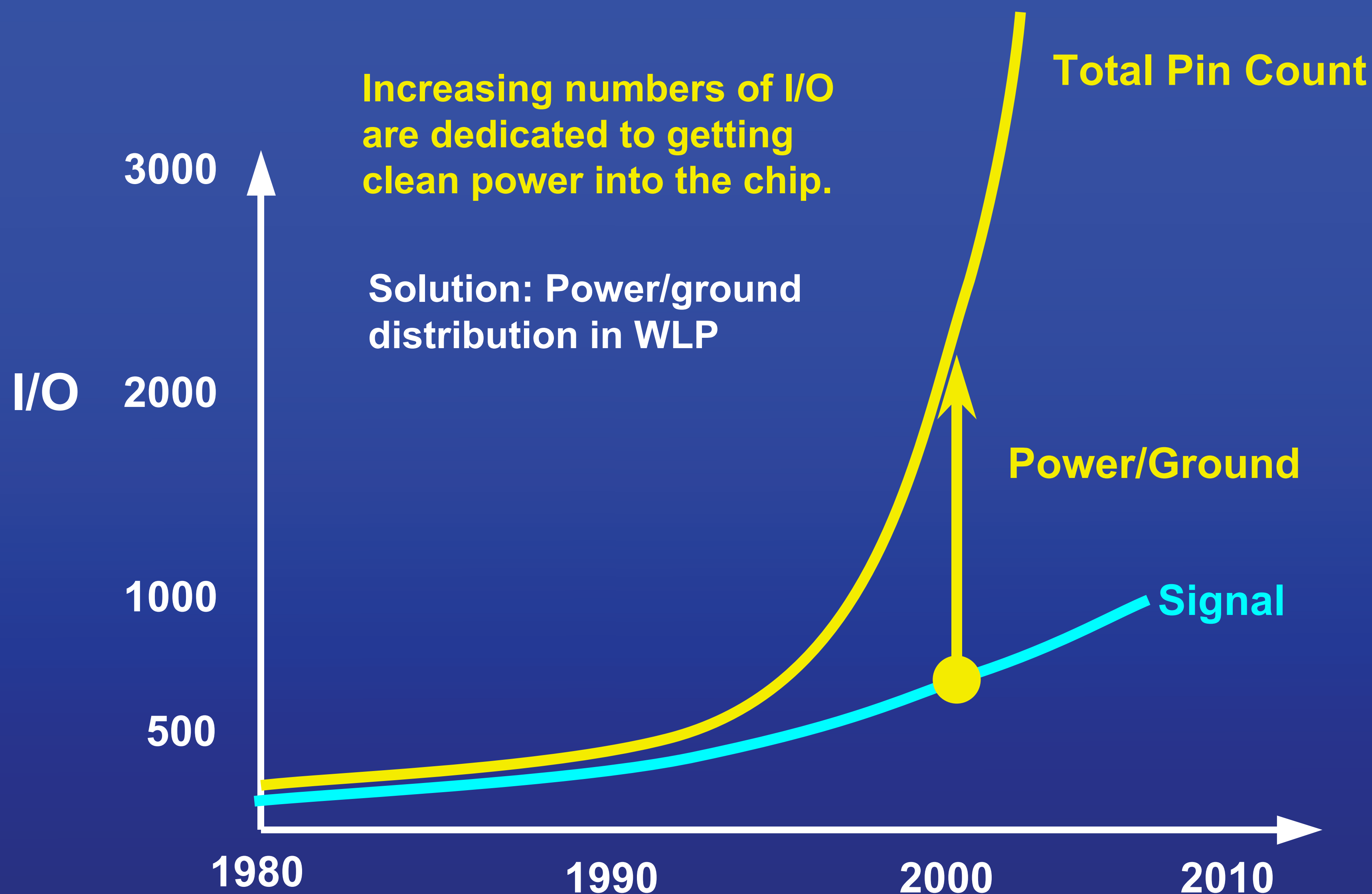
Copper/Invar/Copper



- **A direction to watch**
  - **Low CTE Substrates**
  - **Via Density**

FUTURES

- Cost
  - Batch Processing
  - Simplified Logistics
- Power and ground distribution
- Global Routing in the IC
- Package Integration for Greater Functionality

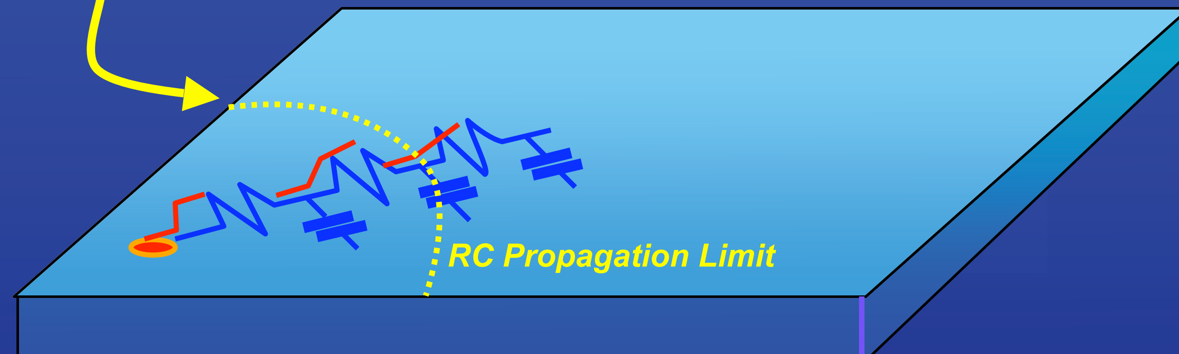

The I/O Explosion
Total Pin Count
Increasing numbers of I/O
are dedicated to getting
clean power into the chip.
Solution: Power/ground
distribution in WLP
3000
I/O
2000
1000
500
Power/Ground
Signal
1980
1990
2000
2010

I/O Explosion: Power/Ground Distribution

- Distribute the Power and Ground on Chip
  - Better electrical characteristics
  - Shorter distance to the shielding planes
  - Dramatically reduces I/O connections for power/ground
    - *80+% of I/O on advanced processors is Power/Ground.*
- Power and Ground Layers on the Wafer
  - Efficiency of production
    - *Avoid paying for large number of power/ground pins.*
  - Makes the chip easier to test - fewer power/ground contacts

RC Delays on Chip Limit Performance

RC Waveform Distortion Limits Propagation to ~ 2mm at 0.18μ

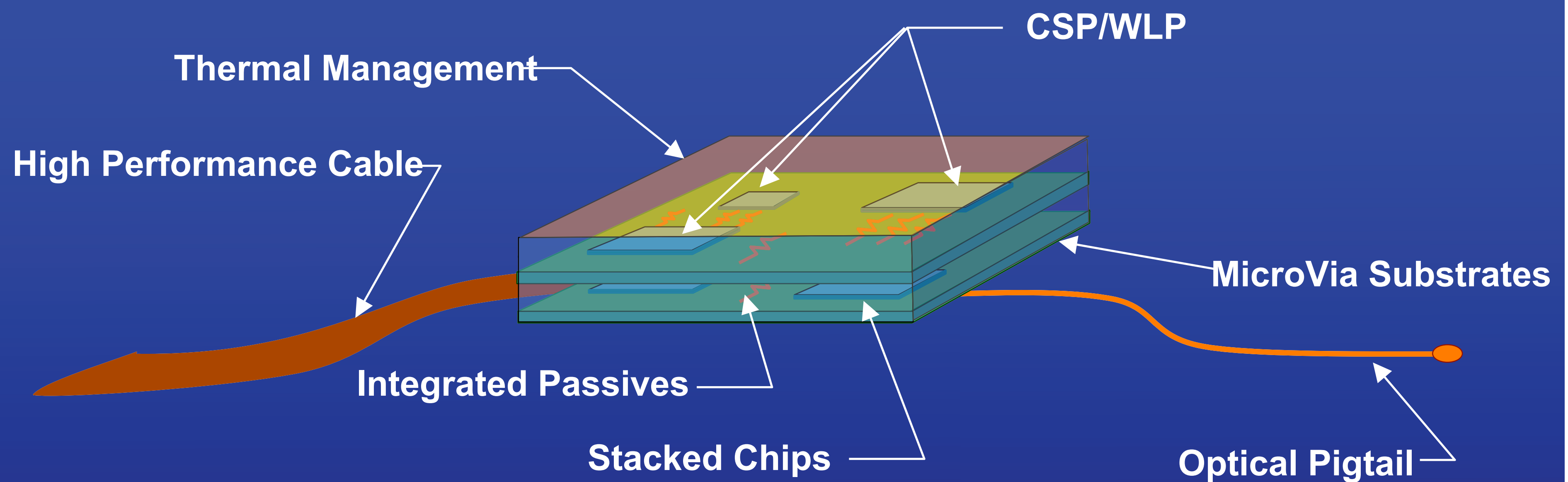


Solution: High Performance WLP Interconnect Reduces RC Delays

Package Wiring Enhances IC Performance

- Global Distribution of High Speed Clock
  - Use high performance nets in the package for clock distribution
- Routing Critical Nets
  - Low resistance copper nets provide low RC delays for long net runs
- The RC delay problem increases as technology advances
  - RC scales as resistance -> $(\text{lithographic dimension})^{-2}$

A View of the Future:



Wafer Level Packaging is a Process

- **Improvements drive a learning curve for cost reduction**
- **New processes allow added IC functionality**
- **Infrastructure is needed to go mainstream**
  - **Test and burn-in**
  - **High density printed wiring boards**