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Wafer Level Packaging — Today's Realities and Future Potential

Wafer level packaging (WLP) offers an exceptional promise: chip packaging can provide learning curve productivity gains like those enjoyed by the integrated circuit industry for the past half century. Not surprisingly, WLP appeared soon after an enabling Chip Scale Package exploded into view.

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The nearly unfathomable productivity gains in integrated electronics underlie most of the advances, and indeed the structure of our modern world. Without ICs, our cell phones, internet, high speed communications, and much more would not exist. These unprecedented gains, characterized in Moore's law[1], flow from the efficiency of processing of large numbers of devices in parallel. All this would be impossible if transistors were assembled, one-at-a-time, like an old 2N109 transistor that some of us still remember.

While the integrated circuit has made monumental advances over the past half century, the fundamental elements of packaging technology have changed relatively little until recently. Now, Wafer Level Packaging offers an exceptional promise: chip packaging can provide learning curve productivity gains like those enjoyed by the integrated circuit industry for the past half century. Not surprisingly, WLP appeared soon after an enabling Chip Scale Package exploded into view. With the CSP, the package can fit under the shadow of the chip, allowing the CSP to be fabricated directly on the wafer (WLP). In principle, Chip Scale Packages can be fabricated in parallel by wafer processing rather than by conventional assembly techniques. WLP offers more interconnections, ground planes, power planes, embedded components and functionality at progressively lower costs. Wafer Level Packaging is a parallel processing paradigm applicable to a range of packaging technologies for fabricating part or all of a package directly on a wafer. It does not connote a specific package or packaging technology, but rather can be applied to all CSPs.

Wafer Level Packaging has already been applied a diverse set of applications and packages, primarily for packages less than 50 pins. As an indication of the promise of the WLP sector, TechSearch International forecasts[2] a 14% growth (CAGR) over the years 2007-2014. The projected growth is driven by form factor, performance, and cost. Beginning from a base in small analog and communications chips, WLP is making inroads into sensors, camera chips, clock generators and other MEMS devices. A prodigious level of integration is achieved in the more advanced MEMS applications such as the Tessera wafer level camera chip. This is a field very much in its infancy, with great promise in the future for higher levels of integration and performance.

A new wave of IC packaging technology sweeps through the industry about every two decades. It is instructive to review the development of IC packaging families represented in **Figure 1**. The driving force for each wave is simply the demand for greater density -more chip interconnections per unit volume. Of course, designers always want as much density, performance and function as possible. However, the cost of building the manufacturing infrastructure for a new packaging family is staggering – and not changed overnight. Timing of each new wave is limited by the investment cycle for new infrastructure in a low margin, capital intensive industry. Because of the long payback period, the IC packaging industry can afford to bring in a pervasive new technology about every two decades. We are

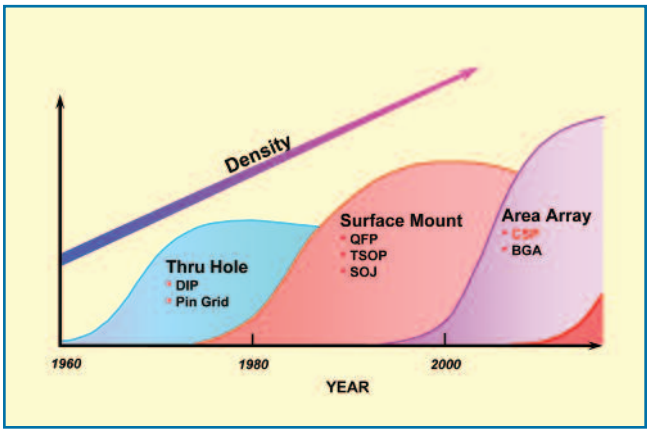

Figure 1. Tracking the development of IC packaging families and increased IC density

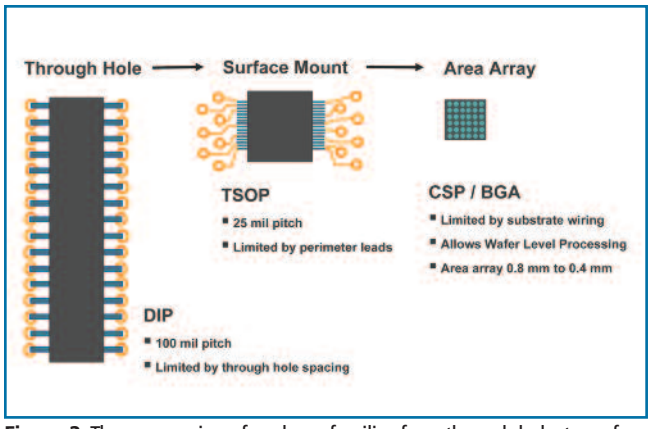

Figure 2. The progression of package families from through hole, to surface mount, and then area array contacts

now well into the build-out of infrastructure for area array packaging, as exemplified by the CSP.

Regarding practical aspects of the last several waves of technology, each was driven by a need to make more electrical contacts to a chip. Simplified to its essentials, **Figure 2** illustrates the progression of package families from through hole, to surface mount, and then area array contacts. The density of through hole connections is limited by PTH spacing on the board. Surface mount overcomes this limitation by soldering leads to pads on the circuit board, eliminating the need for a PTH for every lead. Surface mount is limited, in turn, by the number of leads that can be arrayed easily around the package perimeter. Area array packaging overcomes this limitation by arraying the contacts on a package substrate under the chip in a Ball Grid Array. Why not place all of the contacts on a high density grid array directly under the chip? Such high density packages could be fabricated, but applications are limited by wiring capability of low cost substrates to grids of 0.5 mm and greater. Clearly, area array packaging is progressing toward CSP at a rate limited by circuit board and socket infrastructure to support high density grids at commodity pricing. This move toward CSPs greatly facilitates adoption of the wafer level paradigm for process based fabrication of packages.

One might reasonably ask, 'If we have a new wave of packaging every 20 years, what's next?' Likely candidates are already on the playing field, but it is still early. For increased density, we will eventually get to three dimensional structures, particularly for memory modules. Virtually every memory manufacturer, DRAM and Flash, is exploring Through Silicon Vias (TSV) for chip stacking. Further, stacked package technologies of various types and applications are being explored intensively in laboratories around the world. Regardless of which technology emerges as the next wave of packaging, it will involve wafer level processing. Certainly, TSV chips may be fabricated, tested and finished on the wafer, ready for dicing and assembly into modules. WLP techniques will be used in the fabrication of this and succeeding waves of packaging technology. It is important to make the distinction that WLP is not a package technology, but rather it is a processing paradigm applicable to all future packaging technologies, regardless of the specific type.

WLP is well entrenched in packaging of small ICs for applications in power conditioning, analog, rf-communications and microcontrollers. Early WLP examples were little more than flip-chips dressed up as packages, limited in size to about 3-4 mm as indicated by falling within the blue domain of **Figure 3**. For die sizes larger than about 4 mm, the reliability of solder attachment to CTE mismatched circuit boards is a problem to a greater or lesser degree, depending upon underfill and solder type. In the vertical direction, pin count is limited due to the wiring capabilities of commonly available circuit boards. Grid pitch is currently at 0.5 mm or greater, with an emerging capability for 0.4 mm. Recent advances[3] on the eWLP by Infineon will further extend the WLP domain to larger die sizes and pin counts. However, important applications in memory and processor chips still lie outside the WLP domain, although it is in these areas that WLP has most to offer.

While it has made rapid progress in small chip applications, Wafer Level Packaging has yet to go mainstream. Memory manufacturers continue to work at solving the remaining problems of getting WLP memory into the market. Two roadblocks stand in the way: cost-effective solutions to reliable solder attachment and wafer burn-in. While many low cost technologies are used for solder attachment of small chips, they do not offer acceptable reliability at large DRAM die sizes. Solder columns, copper posts, metal coated polymer balls, solder bumps, and the like accommodate thermal mismatch by plastic deformation that entails a fatigue failure mechanism that scales as a power of the die size. The DRAM environment outlined in **Figure 4** illustrates the status, where reliable attach technologies are expensive in terms of manufacturing cost and infrastructure investment required. Low cost alternatives are available but not proven. Progress continues to be made with the likely prospect that a cost-effective solution will emerge from the mix. One approach is to sidestep the problem by using a low CTE substrate for the memory module, thereby lessening ther-

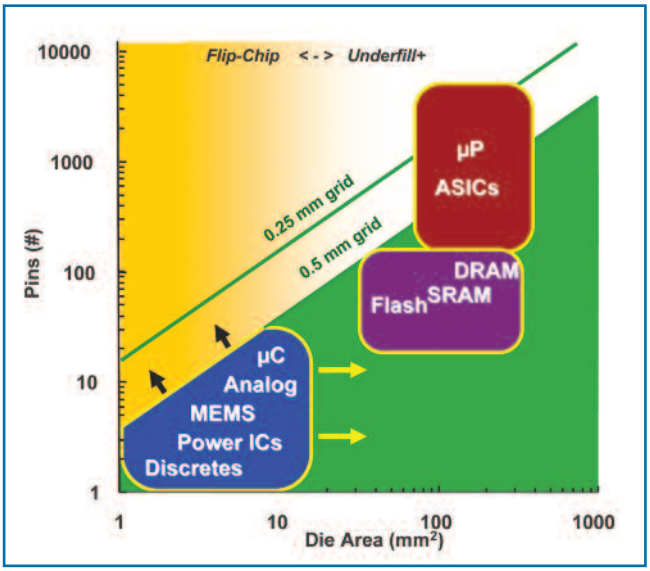

Figure 3. Early WLP examples were little more than flip-chips dressed up as packages, limited in size to about 3-4 mm as indicated by falling within the blue domain shown

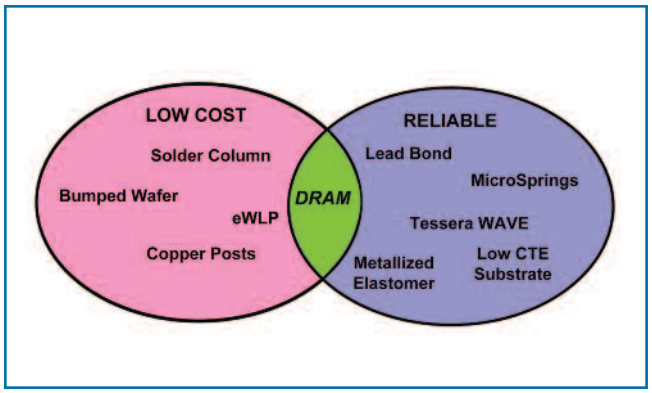

Figure 4. DRAM environment illustrates the status where reliable attach technologies are expensive in terms of manufacturing cost and infrastructure investment required

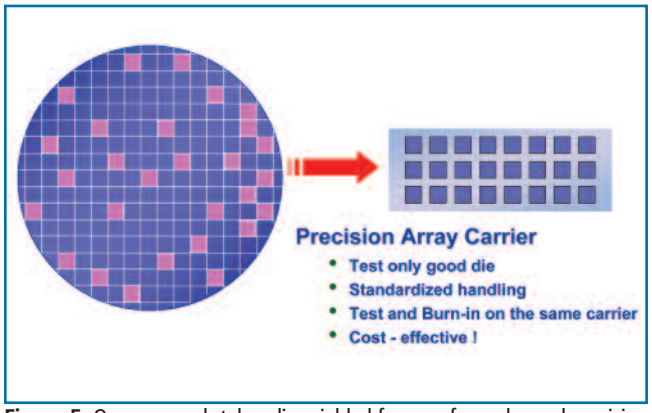

Figure 5. One approach takes dice yielded from wafer probe and precision loads them into a precision array carrier

mal mismatch and improving reliability. These problems are not insoluble.

A second roadblock is a lack of a cost-effective approach to burn-in and final test of WLP DRAM. Full wafer contactors are available at 300 mm, but the existing probe technologies are prohibi- tively expensive for applications in burn-in. The problems are not unlike those of Known Good Die, the nemesis of multi-chip modules. Perhaps the problem of full wafer burn-in may yet be solved, but other approaches are likely to offer a better strategic direction. One approach, outlined in **Figure 5**, takes dice yielded from wafer probe and precision loads them into a precision array carrier. The dice are then transported and contacted for burn-in and for final test. Fully tested parts are marked and then removed from the carrier for shipment. Precision array carriers are suitable as a shipment medium, allowing parts to be unloaded directly into a memory module assembly operation.

In this review of the evolutionary status of wafer level packaging, we have only scratched the surface of the potential applications. In the future, wafer level processing will be used to incorporate significantly more functionality and performance into the IC at on a learning curve characteristic of the semiconductor industry. It is here that the greatest promise of WLP lies. Added functionality such as power and ground distribution can greatly simplify contacts to the chip while improving performance. Global nets such as clock distribution trees can be routed in high performance transmission lines in the package, rather than on RC delay limited lines on the chip as is done today. The prospects are open ended for using the package to integrate functionality into the IC, blurring the distinction between semiconductor and package. WLP can make its most valuable contribution in extending Moore's law further well into the future.

References

1. The original Moore's Law states that the number of devices on a chip doubles every 18 months. Revised in 1970, the Law doubles the number of devices every 2 years.

2. Jan Vardaman, TechSearch International (2008).

3. Dr. Reinhard Ploss, IFX Day 2008 (Munich June 3, 2008).