

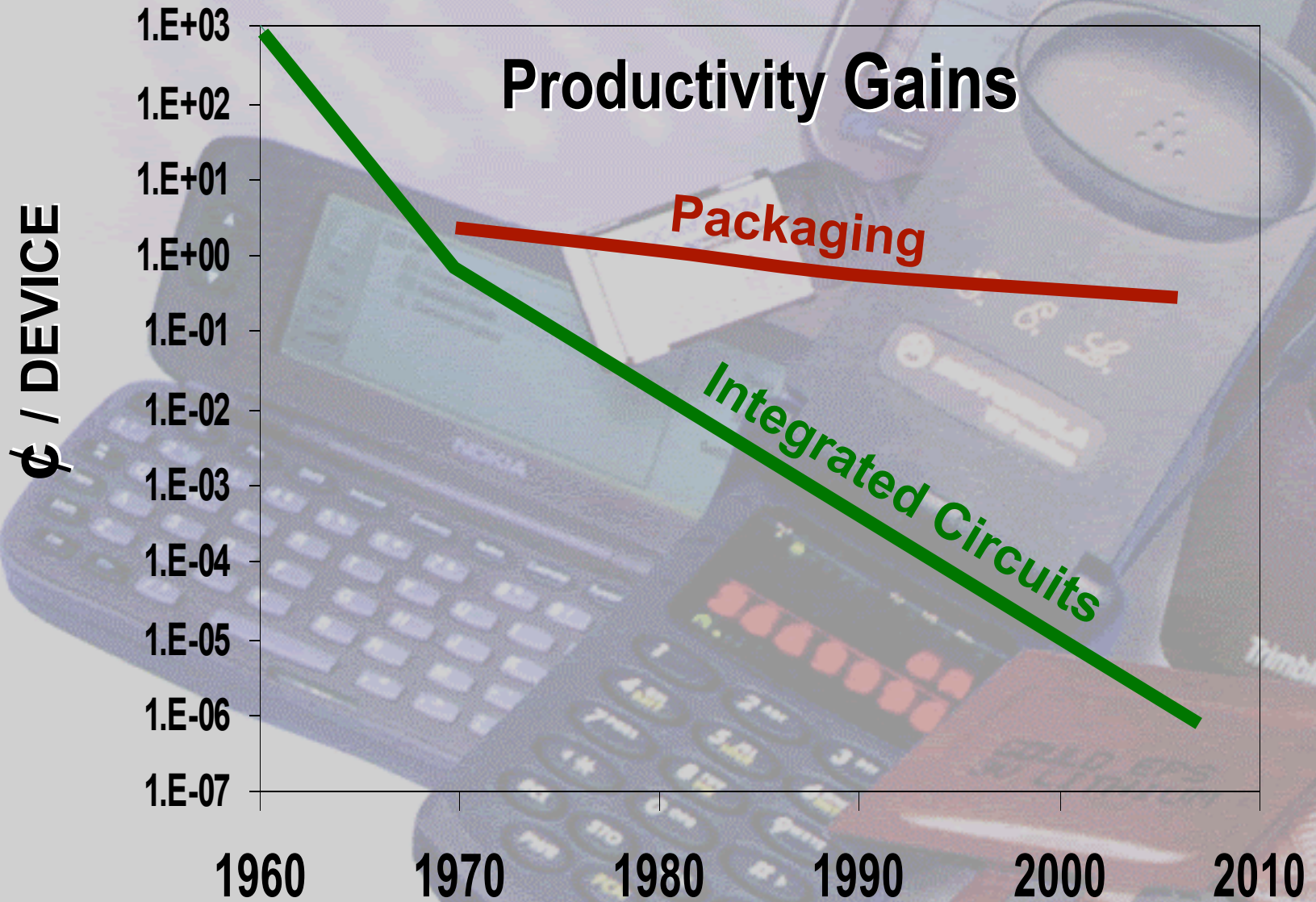
***Wafer Level Packaging  
... The Next Turn in the Road***

***Dr. Thomas Di Stefano  
Centipede Systems, Inc.***

**IEEE CPMT 2009**

# Could back end packaging and test provide productivity improvements like the Moore's Law gains enjoyed by Semiconductor FABs?

- Wafer Level Processing
- Lights Out Automation
- Standard Handling Protocols
- Intelligent Burn-in and Test



# Semiconductor Productivity Gains

## Parallel Processing – More Devices per Wafer

- Increasing level of integration
- Shrinking device dimensions

## Device Improvements

- Increases in Clock speed
- Fewer devices per Cell

## Automation

- Lights out FAB
- Focus on process/tool improvement



## Single Wafer FOU<sup>\*</sup>

- Standard Interface for Full Automation of FAB Front End
- Enables Lights-Out Semiconductor Automation<sup>+</sup>

\* Front Opening Unified Pod

+ Allen Ibara, CEO PhiAm

# Lights Out Automation \*

## Cycle Time

- 50% improvement in two years

## Tool Utilization

- 10-30% improvement in two years
- Re-use of (standard) tools is essential

## Process Learning

- Focus on tool and process instead of moving WIP
- WIP is moved automatically

\* From Tom Franz, VP and GM FAB/Sort Manufacturing, Intel Corp.  
VLSI Research July 25, 2007

# Packaging/Test Productivity

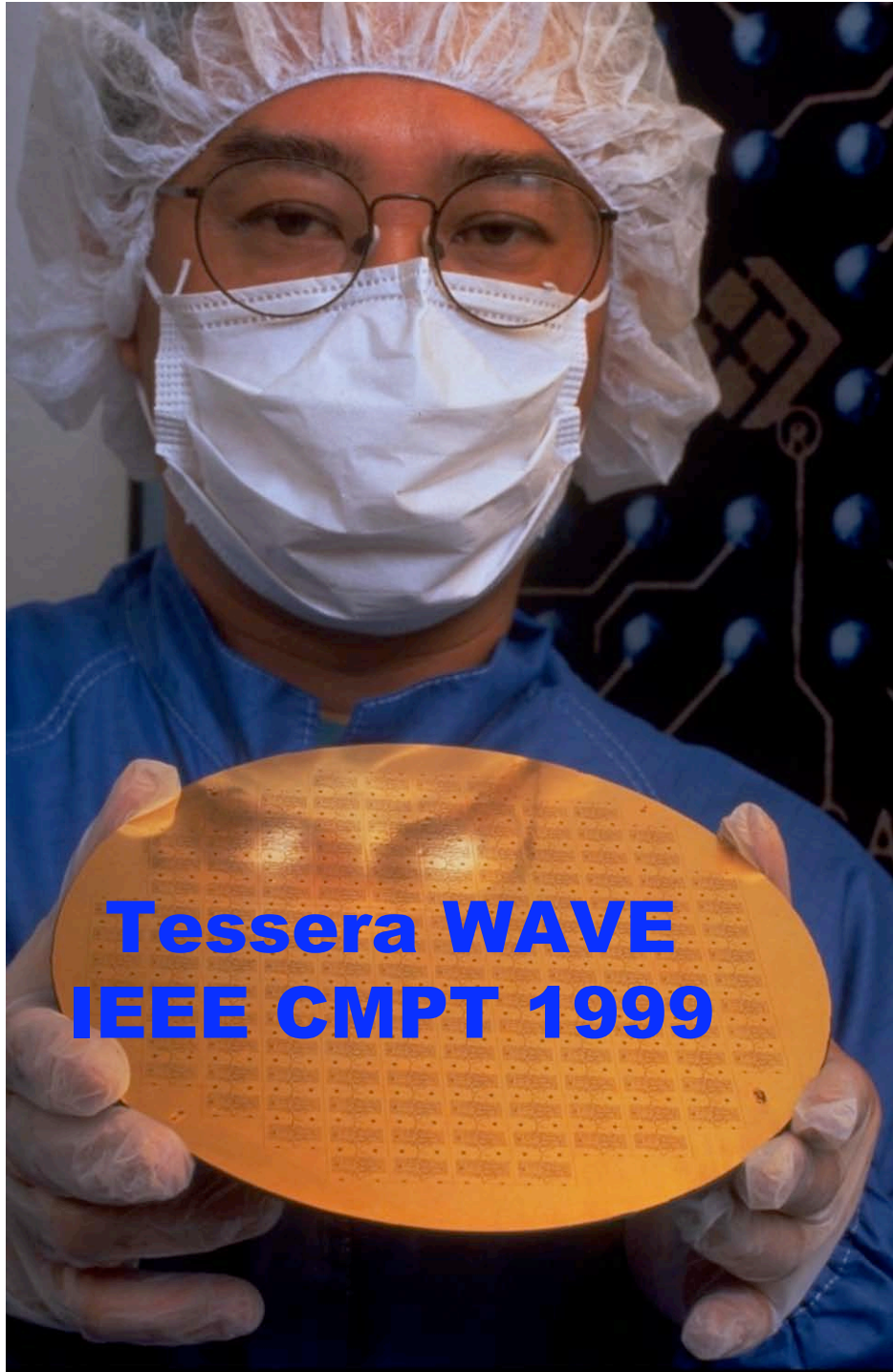
## Relatively Static Cost Structure

- Packaging cost per chip slowly decreasing
- Test costs increase with complexity
- Test and burn-in fixtures
- Lack of standardization
- Mixture of handling and logistics protocols

# Lights Out Automation

## Key Enabling Factors for the Back End

- Wafer Level Packaging Facilitates Automation (FOUP)
- Standard Chip Transport (Tray)
- Test in Tray (TNT)
- Intelligent Burn in (TDBI)



**Tessera WAVE  
IEEE CMPT 1999**

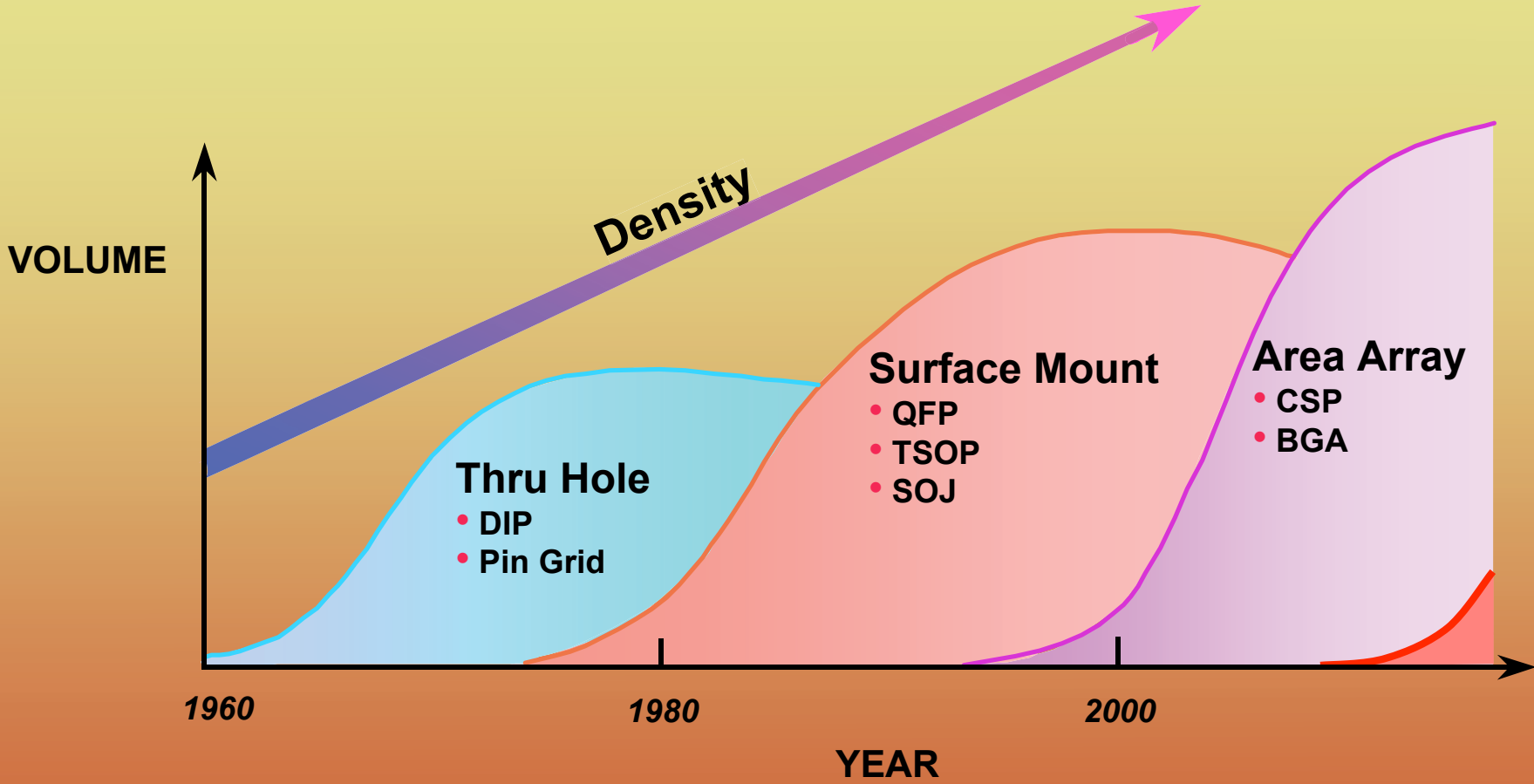
## **WLP 1999**

- **Driven by Size/Performance**
- **Solder Attach to PCB**
- **Single Chip Applications**
- **Cost Parity**

## **WLP 2009**

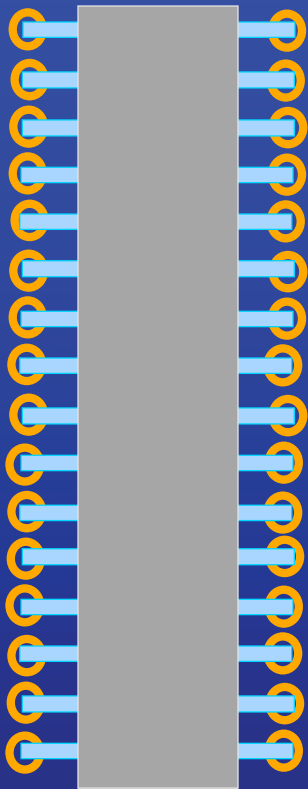
- **Driven by Cost**
- **Through Silicon Via Option**
- **SiP and Stacking Applications**
- **Integrated Processing**

# CSP-WLP Enables New Wave of I/O Density



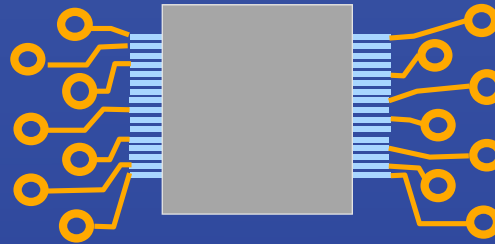
# IC Packaging Progression:

Through Hole → Surface Mount → Area Array



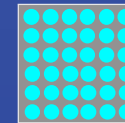
**DIP**

- 100 mil pitch
- Limited by through hole spacing



**TSOP**

- 25 mil pitch
- Limited by perimeter leads



**CSP / BGA**

- Area array 0.8 mm to 0.3 mm
- Limited by substrate wiring
- Allows Wafer Level Processing

# WLP Enjoys Exceptional Growth

## TechSearch Projects 14% Growth (CAGR) for 2007 - 2014

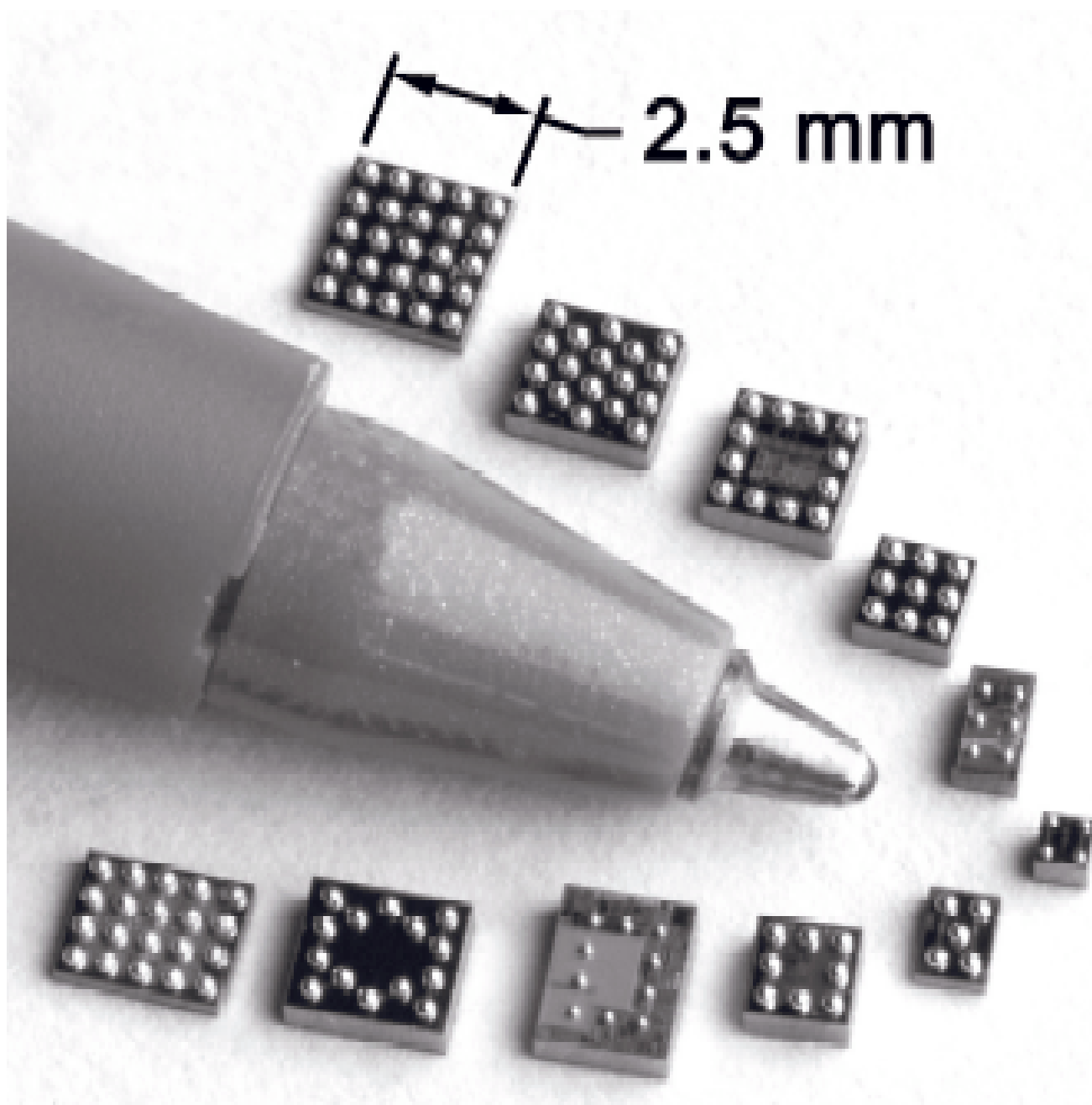
- Diverse set of applications & technologies
- Growth concentrated in packages < 50 pins
- Driven by performance, form-factor (...AND COST!)

## Growth in Wafer Level Packaging of MEMS Devices

- Camera chips
- Pressure sensors
- Crystal Oscillators, ...

## Emerging Applications in Through Silicon Via (TSV)

- Stacked memory



2.5 mm

# Micro-SMT

National Semiconductor

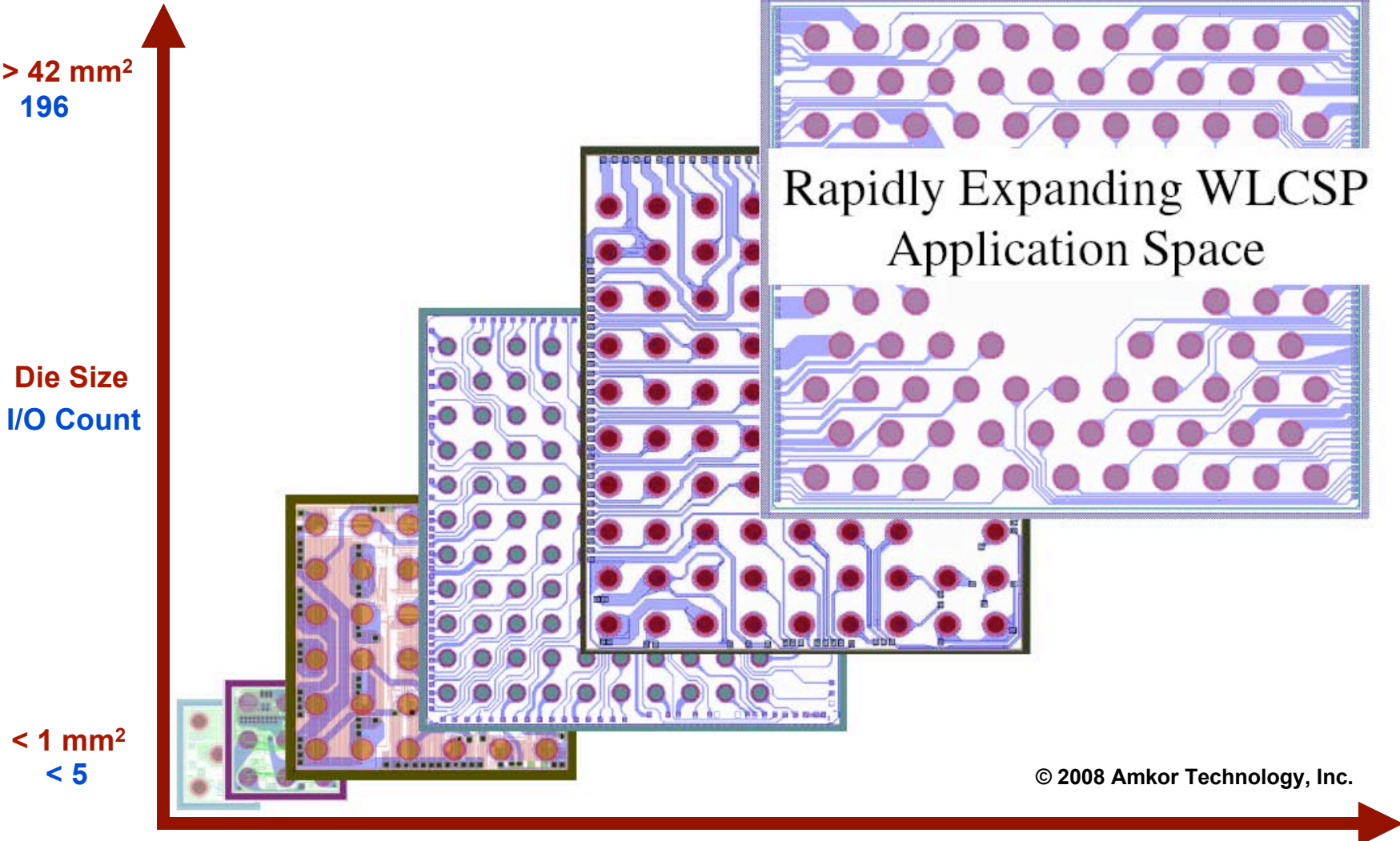
## WLCSP Market\*

- **Strategic and rapidly growing WLCSP business**
- **> 1.3 Billion WLCSP's shipped since 2005**
- **>95% of WLCSP's shipped include RDL and lead free solder bumps**
- **Multiple customers in production, wide range of new designs in qualification**
  - 0.5mm pitch dominant
  - 0.4mm pitch emerging
  - 0.3mm pitch in development
- **First 300mm WLCSP qual achieved in T5 as of October 1, 2006**
- **Global wafer level process manufacturing footprint**
  - 7 countries and 15 sites

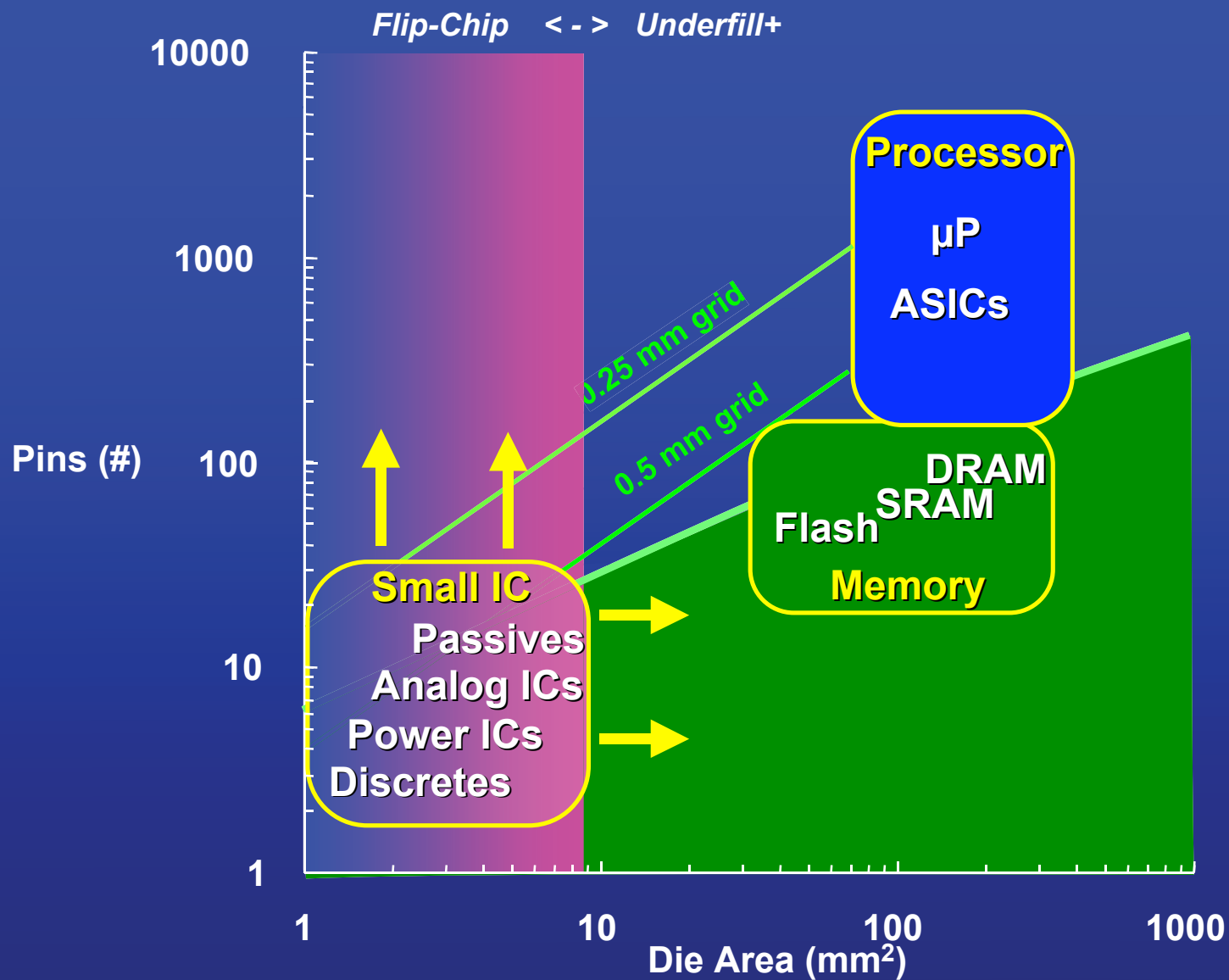
\* From Lee Smith, Amkor

© 2008 Amkor Technology, Inc.

# Expanding WLCSP Application Space



© 2008 Amkor Technology, Inc.



# Wafer Level Packaging

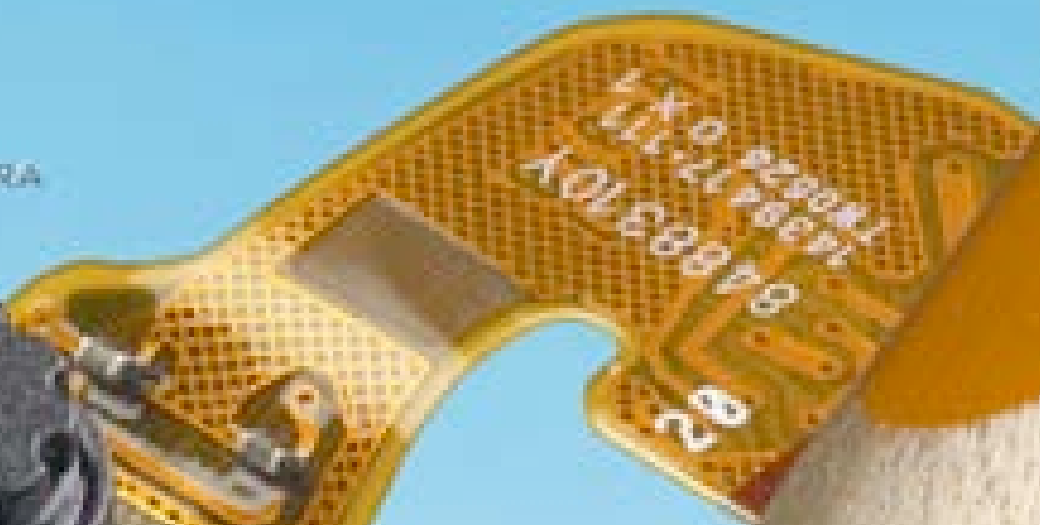
## Utilizes Processing to achieve lower costs

- Wafer Processing
- Wafer Handling and Automation
- Industry Standards

## WLP is not a specific packaging technology

- Small bumped die
- MEMS
- Through silicon via
- Stacked Chips
- ...

CONVENTIONAL CAMERA  
MODULE



To SCALE

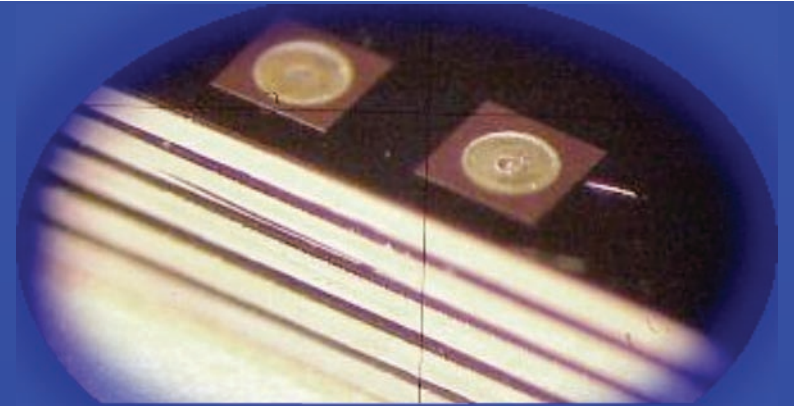
**Tessera iWLC**

## **WLP has not gone Mainstream (i.e. DRAM)**

- **Reliable Solder Attach Technology**
- **Cost Effective Wafer Burn-in and Test**
- **Cost!**

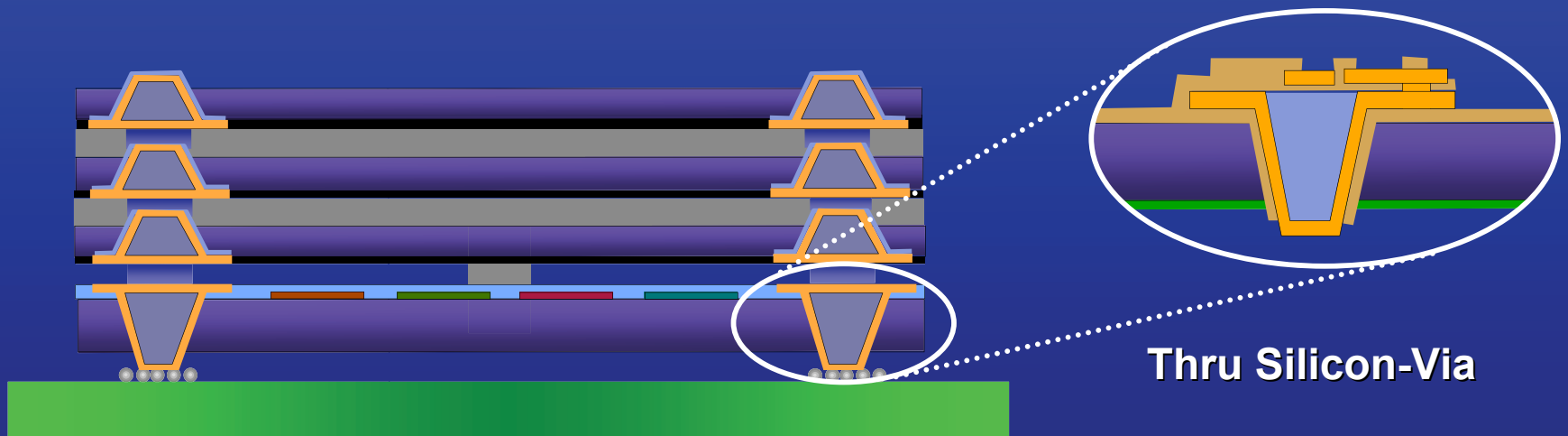
## **Recent developments could change the game**

- **SiP relaxes thermal mismatch problem**
- **TSV allows stacked chips**
- **Intelligent burn-in and test**
- **Automation Standards**



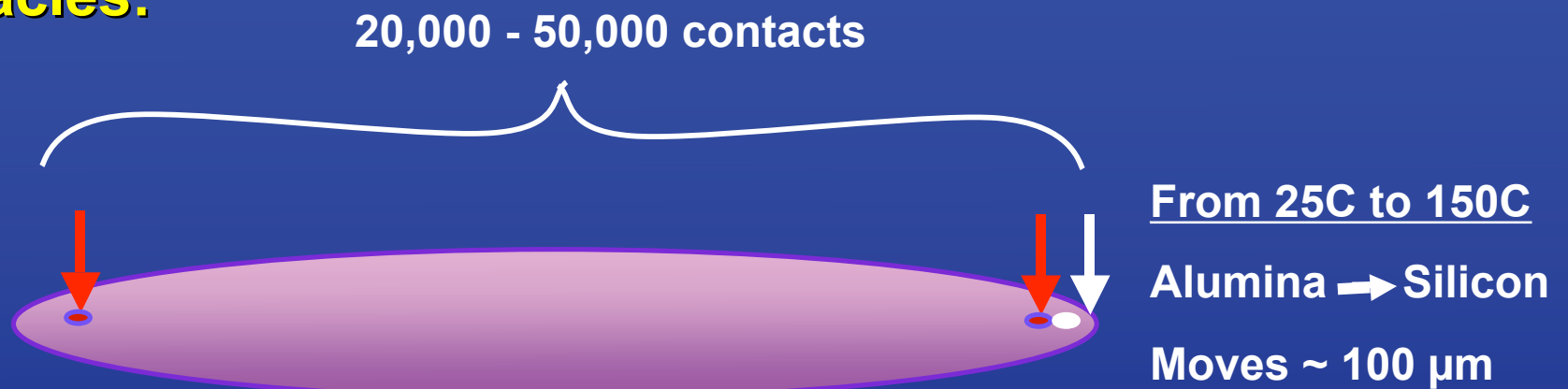
COURTESY ALLVIA

# TSV (Thru-Silicon Via)



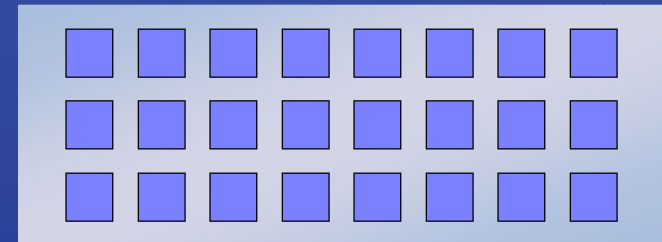
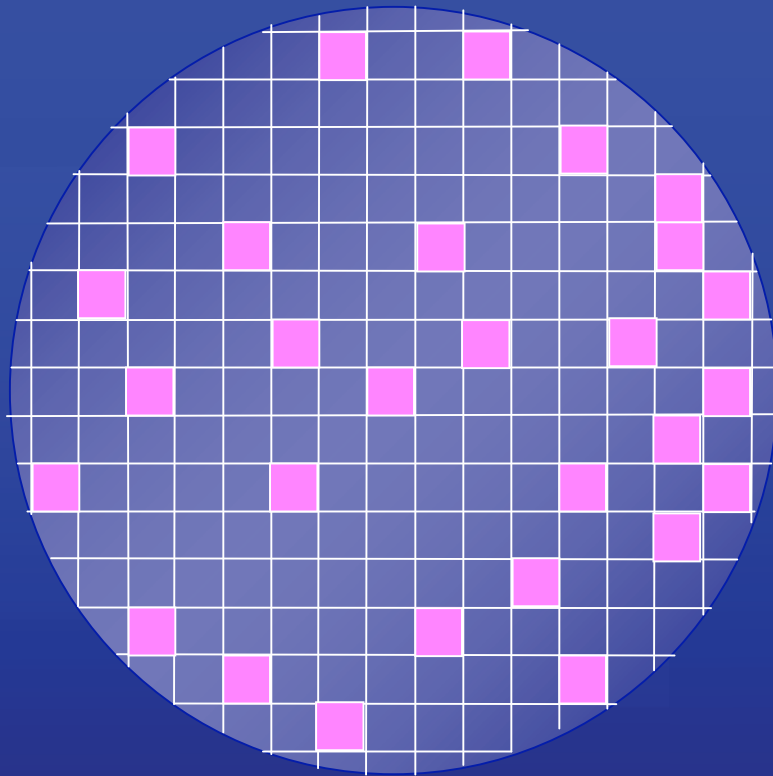
# Full Wafer Burn-in ??

## Technical Obstacles:



**Cost:** Must cost  $\ll$  \$50,000  
Equivalent to burn-in sockets & boards.

# Automated Handling for Test and Burn-in

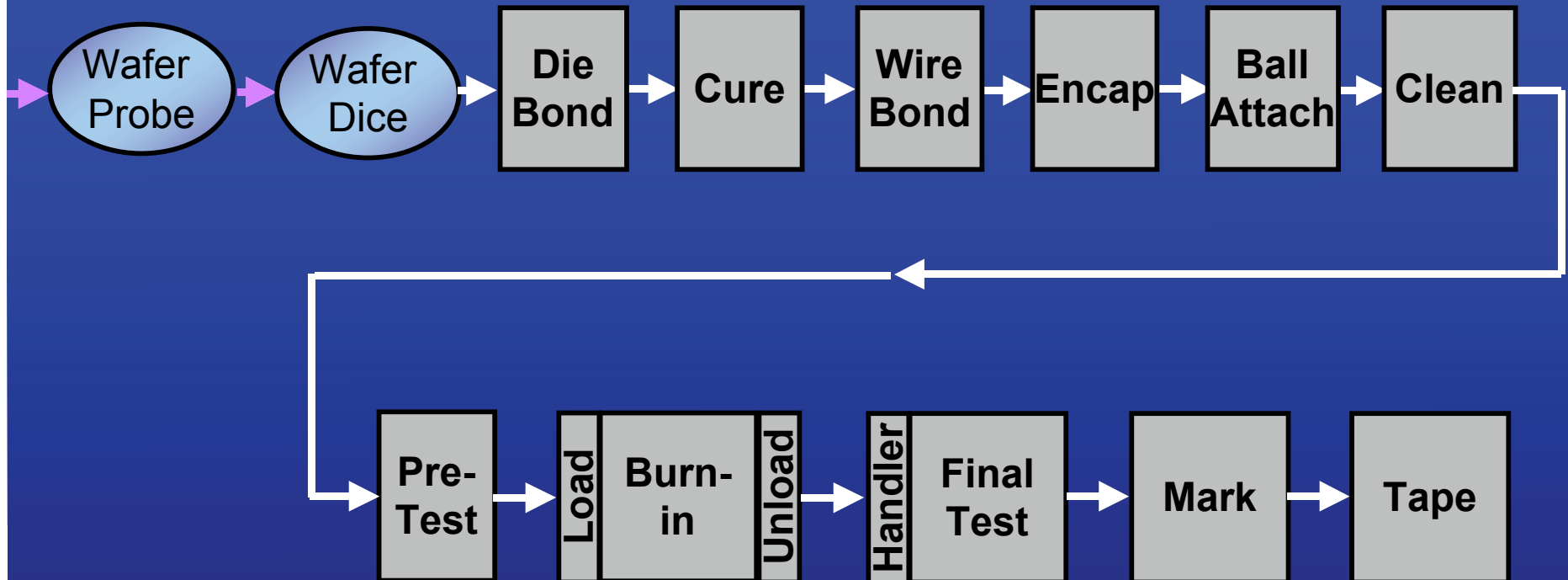


- **Test-in-Tray**

- Test only good die
- Standardized handling
- Test and Burn-in on the same tray
- Cost !

## Traditional Back End

- Many different fixtures and “standards”
- *Ad Hoc* agglomeration of handling protocols



→ FOUP Transport

# Test in Tray (TNT)

## Automatic handling of parts through the entire process

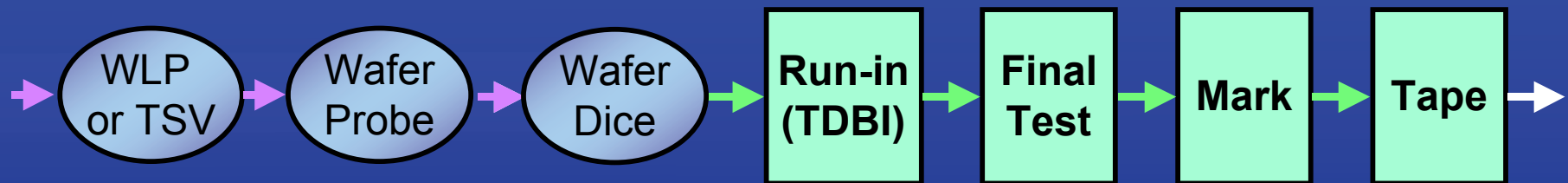
- Standardized trays
- Automated Burn-in
- Test at temperature
- Post test processing
- Potential for Lights Out Manufacturing



## Test in Tray (TNT)

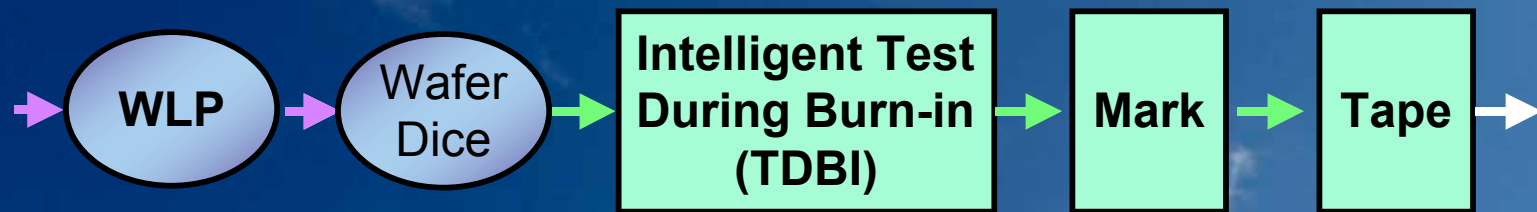
- Standardized Format
- Fully Automatic Handling
- Parts Stay in Tray Throughout Back End
- Burn-in, Test, Mark, Clean and Pack
- All Device Types

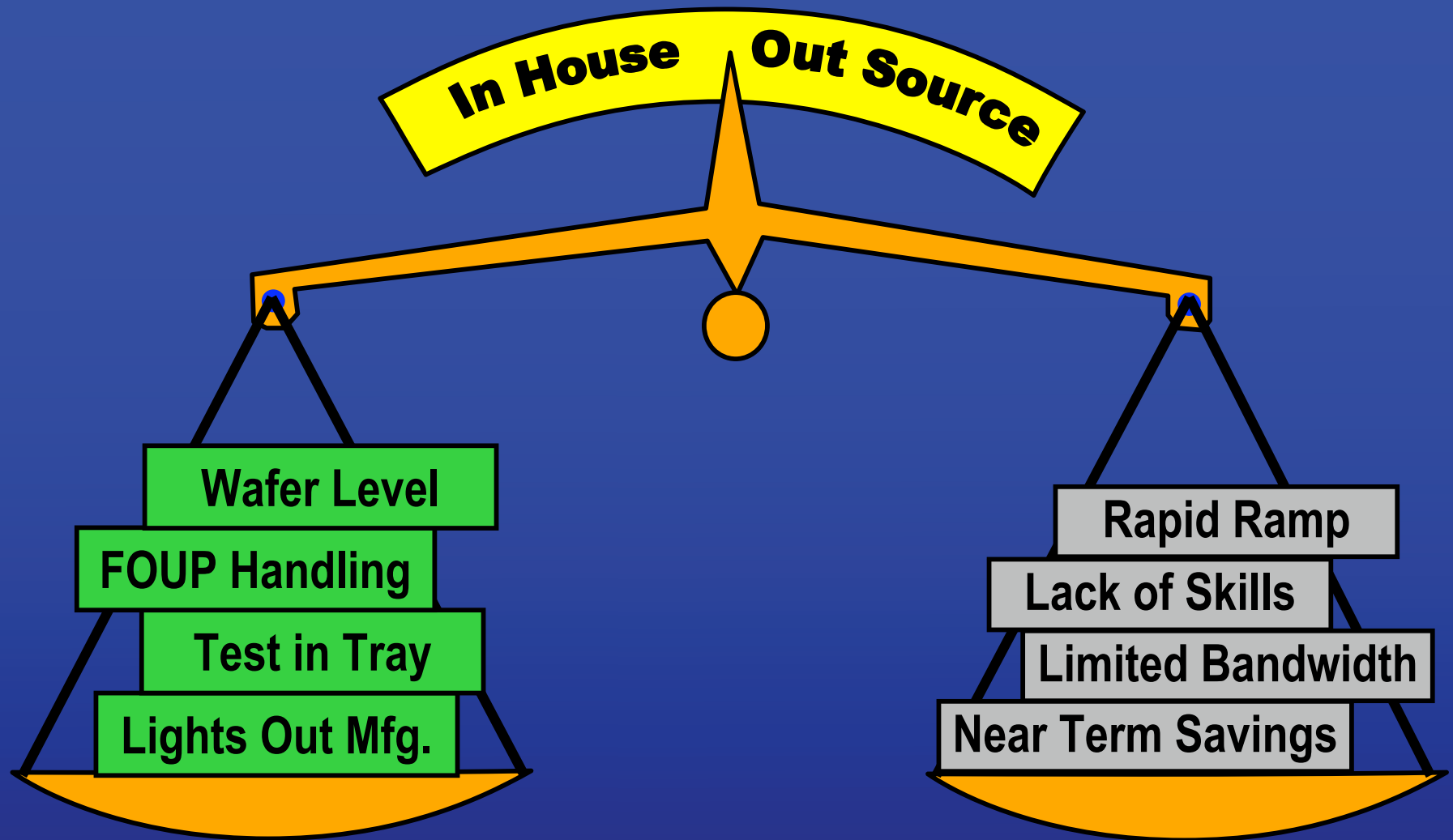
# Integrated Back End



Lights Out Automation = FOUP Transport + TNT Transport

## A Bit of “Blue Sky”





Outsource if you have no IP to protect

# Wafer Level Packaging

Packaging and Test can Contribute to Productivity



- **Wafer Processing of Package Components**
- **Automation of Wafer Handling (FOUP)**
- **Test in Tray (TNT)**
- **Intelligent Burn-in and Test**
- **Lights out Factory**